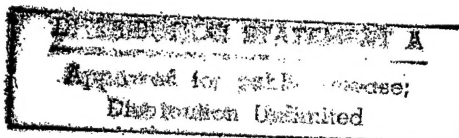


# Final Technical Report

## Defects and Impurities in 4H- and 6H-SiC Homoepitaxial Layers: Identification, Origin, Effect on Properties of Ohmic Contacts and Insulating Layers and Reduction

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13. ABSTRACT (Maximum 200 words) Page 2 of 2 <p>(<math>1.8 \pm 0.4</math>)<math>\times 10^7</math> V/cm were determined for Chynoweth's equation for 6H-SiC and 4H-SiC, respectively, at room temperature. The coefficient <math>a_p</math> was found to decrease with increasing temperature for both polytypes while the coefficient <math>b_p</math> remained constant. Based upon this data, the breakdown voltage of the 4H and 6H-SiC devices is predicted to increase with temperature which is an important desirable characteristic for power devices. The electrical characteristics of lateral n-channel MOSFETs fabricated on 4H-SiC are reported for the first time. Inversion layer electron mobilities of 165 cm<sup>2</sup>/V-s in 4H-SiC MOSFETs were measured at room temperature.</p> <p>Tantalum deposited on p-type 6H-SiC(0001) showed good diode characteristics with low reverse leakage currents to 350°C (~5<math>\times 10^{-7}</math> A/cm<sup>2</sup> at 5 V). Current transport across the interface is dominated by thermionic emission only at temperatures above 300°C. The ideality factors decreased from 2.24 at R.T. to 1.07 at 400°C. Schottky barrier heights (SBH's) calculated from these measurements are underestimated for the lower temperatures, where current transport is believed to be dominated by recombination. Similar contacts on n-type 4H-SiC also displayed good diode behavior at 25°C with significant increases in reverse leakage at temperatures as low as 100°C. TaC on lightly doped (4.1<math>\times 10^{16}</math> cm<sup>-3</sup>) n-type SiC resulted in leaky diodes at R.T; they exhibited ohmic behavior at T &gt; 200°C. The same contacts on p-type (2<math>\times 10^{15}</math> cm<sup>-3</sup>) material displayed diode behavior with low reverse leakage currents to 250°C. Good reversibility of the current-voltage characteristics of all of these contacts after cycling between R.T. and 400°C was observed. These results indicate the absence of interfacial reactions and, hence, the potential for thermally stable contacts to 400°C.</p>					
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## I. Introduction

The two most important materials-related problems affecting the performance of all SiC devices and their associated components (e.g., contacts) are the defects and the undesired impurities which become incorporated in the homoepitaxial SiC layers in which all devices are currently fabricated. Bhatnagar [1] has shown that the reverse blocking leakage current in high voltage Schottky diodes is three orders of magnitude higher than theoretically predicted as a result of defects in the epi-layer. The formation of micropipes, stepped screw dislocations, interacting dislocation loops, polyganized networks of dislocations and growth twins as well as stacking faults during the sublimation growth of SiC boules are likely the root cause of some of the defects in the epitaxial layer. However, with the exception of the micropipes, the types and concentrations of line, planar and other three-dimensional defects and their effect on the performance of devices and individual device components in the important epi-layer have not been similarly determined. As such, it is not known which of the latter defects actually are translated from the wafer into the epi-layer during its deposition and, therefore, should be vigorously controlled during boule growth and which defects are generated during deposition.

The relatively uncontrolled occurrence of the n-type donor of N and deep level compensating impurities such as Ti in the epilayer have been identified via secondary ion mass spectrometry, photoluminescence and cathodoluminescence investigations. However, the origins of essentially all of these impurities are unknown. For high-temperature, -power and -frequency devices, it is highly desirable to control or eliminate these impurities such as to attain undoped films with uncompensated carrier concentrations of  $10^{14} \text{ cm}^{-3}$ —two orders of magnitude lower than what is, at present, normally achieved in standard commercial depositions.

The formation of low resistivity and thermally stable ohmic contacts to 4H- and 6H-SiC remains a serious problem in the development of SiC device technology. For SiC power devices to have an advantage over Si, the contact resistivities must be below  $1 \times 10^{-5} \text{ W-cm}^2$ , as noted by Alok, *et al.* [2]. In addition, the electrical characterization of state-of-the-art SiC films depends on the ability to fabricate ohmic contacts on material with low carrier concentrations. Therefore, better ohmic contacts are needed both for improving device performance and for improving the quality of films which can be grown. The thermal stability of ohmic contacts is of particular concern for p-type SiC, which have traditionally relied on low melting point Al or Al alloys to dope the SiC surface below the contacts. These materials are not suitable for devices intended for high-temperature operation. While the fabrication of ohmic contacts to SiC has also normally depended on the attainment of a very heavily-doped near-surface region, the introduction during deposition of high levels of dopants in the near surface device region of the epi-layer prior to the deposition of the contact or by ion implantation through the contact makes probable the introduction of point and line defects as a result of the induced strain in the lattice.



Based on all of these issues and recent experiments already performed at NCSU, our goals are to produce contacts which are thermally stable and have low contact resistivities while also reducing the need for doping by ion implantation.

To fabricate most microelectronic devices, the growth or deposition of stable insulators is needed to provide both passivating layers and gate dielectrics. Silicon carbide is almost invariably thermally oxidized, albeit at a slower rate, in the same manner and temperature range that is employed for Si. Most of the previous studies regarding the oxidation of SiC have been concerned with polycrystalline materials. It has been shown by Harris and Call [3] and Suzuki, *et al.* [4] that the (0001) face of 6H-SiC oxidizes according to the same linear-parabolic equation reported for Si by Deal and Grove [5]. The model states that the initial stage of oxidation is reaction rate limited and linear, but becomes parabolic as the diffusion of the oxidant through the oxide becomes the rate limiting factor. Research at NCSU by Palmour, *et al.* [6] has demonstrated that the oxidation process on SiC in wet and dry oxygen and wet argon obeys the linear-parabolic law. Both wet processes had a slower rate than dry oxidation at 1050°C and below. The dry oxides exhibited a very flat surface; in contrast, SEM and TEM revealed that wet oxidation preferentially oxidizes dislocation bands, causing raised lines on the oxide and corresponding grooves in the SiC. It was proposed that the much higher solubility of H<sub>2</sub>O in SiO<sub>2</sub> as compared to that of O<sub>2</sub> allows wet oxidation to be preferential.

All of the oxidation studies on all polytypes of semiconductor quality SiC have been conducted on n-type material with the exception of the investigation by Palmour *et al.* [6]. The objective of this study was the determination of the redistribution of the common electrical dopants of N, P, Al and B during thermal oxidation of SiC films at 1200°C in dry O<sub>2</sub>. Experimental segregation coefficients and interfacial concentration ratios were determined. Secondary ion mass spectrometry revealed that B and Al depleted from the SiC into the growing oxide while N and P were found to pile up in the SiC as a result of the loss of the SiC to the oxide formation. Aluminum is now used almost universally as the p-type dopant in SiC. The electrical properties of oxides thermally grown on n-type SiC normally have reasonably favorable characteristics of high breakdown voltage and low leakage currents. However, the reverse is true for thermally grown oxides on p-type SiC, as shown by Baliga and his students at NCSU. It is believed that at least two of the causes of the poor performance on a p-type material are the existence of the Al in the oxide and at the oxide/SiC interface and the dangling oxygen bonds which this species creates in the oxide as a result of a difference in oxidation state (+3) compared to that of Si (+4) and the existence of C at the SiC/insulator interface. Methods of effectively cleaning SiC surfaces prior to oxidation to deposit and grow oxides on p-type material under UHV conditions and determine the effect of Al redistribution and C concentrations at the interface on the properties of the oxide must be determined. In addition,

the effect of existing line and planar defects in the SiC epi-layer on the properties of the thermally grown and deposited oxide must be ascertained.

The research conducted in this reporting period and described in the following sections has been concerned with the (1) phonon scattering limited mobility in SiC inversion layers, (2) role of defects in producing a negative temperature dependence of breakdown voltage in SiC, (3) temperature dependence of hole impact ionization coefficients in 4H- and 6H-SiC, (4) lateral n-channel inversion mode 4H-SiC MOSFETs, (5) electrical characteristics of Ta and TaC Schottky diodes on n- and p-type SiC as a function of temperature, and (6) the valence band maximum at Si/6H-SiC and SiO<sub>2</sub>/6H-SiC interfaces. The following individual sections detail the procedures, results, discussions of these results, conclusions and plans for future research. Each subsection is self-contained with its own figures, tables and references.

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## II. Phonon Scattering Limited Mobility in SiC Inversion Layers

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Lateral MOSFETs were fabricated on SiC using an annealed LPCVD oxide as gate dielectric. The measured inversion layer mobility was studied as a function of device orientation, effective semiconductor surface field and temperature. Process splits were designed to determine the critical thermal cycles that the gate dielectric was subjected to. In this paper we observed that the high temperature  $N^+$  source/drain implant activation anneal at  $1250^\circ\text{C}$  as well as the interface thermalization at  $1100^\circ\text{C}$  were required to obtain high values of inversion layer mobility on SiC lateral MOSFETs. There was no significant dependence of the inversion layer mobility on the azimuthal orientation of the MOSFET to the wafer flat. At higher temperatures and fields, a negative temperature dependence of inversion mobility was observed for the first time in SiC indicating the dominance of phonon assisted scattering processes. At room temperature and at low fields, coulombic scattering was dominant with a positive temperature coefficient. In the negative temperature dependence regime, the measured mobility was found to have a temperature dependence of the form  $T^{-\alpha}$  with  $\alpha$  having a value of about 1 for 6H-SiC and about 1.5 for 4H-SiC. The measured mobility was also found to have a field dependence of the form  $E^{-\beta}$  with  $\beta$  taking values from 0.22 to 0.28. These values for  $\alpha$  and  $\beta$  are close to values measured on silicon inversion layers dominated by acoustic phonon scattering.

## A. Introduction

Silicon carbide MOSFETs have been projected to be very attractive as switches for applications in the 500-1000V range [1]. The fabrication of high performance MOSFETs requires a high quality gate dielectric with good interface properties with the semiconductor. The gate dielectric most commonly employed in SiC is thermally grown  $\text{SiO}_2$  [2-5]. Accordingly, the growth and characterization of thermal oxides on both N-type and P-type SiC (both 6H and 4H polytypes) has been given great importance. However, deposited oxides have also been considered as alternative high quality dielectrics.

Lateral MOSFETs have been previously reported on 6H-SiC by other groups [2-5]. These devices typically had thermally grown gate dielectrics and were found to operate successfully up to high temperatures and also with low drain leakage currents. Lateral 6H-SiC MOSFETs have also been fabricated using deposited oxides [6] as part of a CMOS technology. The authors opted for a deposited oxide in order to avoid the oxide step that would necessarily result due to the differential thermal oxidation rates on the 6H-SiC epitaxial layer and on the heavily doped implanted drain-source layer. This oxide step could result in electric field-crowding and consequently, oxide breakdown at higher gate biases and temperatures. Due to the very low diffusivity of dopants in SiC even up to  $1500^\circ\text{C}$ , non-self-aligned technologies [5] are also considered for the fabrication of SiC MOSFETs apart from the traditional self-aligned technologies [7] which are typically employed for silicon MOSFETs. The implication of a self-aligned technology is that the gate oxide under the patterned polysilicon gate would be subjected to the drain-source implant activation anneal (typically carried out in excess of  $1200^\circ\text{C}$ ) which would adversely affect the properties of the gate oxide. This is in fact observed on the self-aligned MOSFETs in the form of a negative threshold voltage indicating a high positive oxide charge in these devices. Low inversion layer mobilities of around  $20\text{ cm}^2/\text{V}\cdot\text{s}$  for N-channel 6H-SiC MOSFETs had been reported [3-5]. A significant improvement was obtained by Lipkin *et al.* [2] due to improved oxidation techniques as well as post-oxidation and re-oxidation anneals with a maximum mobility of  $72\text{ cm}^2/\text{V}\cdot\text{s}$ . Inversion layer mobilities on lateral MOSFETs on 4H-SiC were reported for the first time by Sridevan *et al.* [8] High values of inversion layer mobility ( $110\text{ cm}^2/\text{V}\cdot\text{s}$  on 6H-SiC and  $160\text{ cm}^2/\text{V}\cdot\text{s}$  on 4H-SiC) were reported on lateral MOSFETs fabricated on both polytypes. These MOSFETs were intended to characterize the field oxide of the process and hence had an  $8000\text{\AA}$  thick gate dielectric. In this paper, we demonstrate that the use of deposited annealed oxides to obtain high inversion layer mobilities in SiC MOSFETs is viable, by reproducing the process used previously, this time with MOSFETs with gate dielectric thickness of about  $850\text{\AA}$ . We report the influence of the critical steps in the process for the first time. The measured data on the temperature and electric field dependence indicate that phonon scattering limited inversion mobility has been observed in SiC for the first time.

## B. Carrier Scattering

Different types of carrier scattering affect the mobility of electrons in inversion layers. Chief among them are scattering due to lattice vibrations (phonon scattering), scattering due to oxide charges and ionized impurities (coulombic scattering), and scattering due to interface asperities (surface roughness scattering). The effective carrier mobility can be obtained from the mobility due to each of the scattering terms by using Mathiessen's Rule:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{cs}} + \frac{1}{\mu_{sr}} \quad (1)$$

where  $\mu_{eff}$  is the effective mobility,  $\mu_{ph}$  is the mobility term due to phonon scattering,  $\mu_{cs}$  is the mobility term due to coulombic scattering, and  $\mu_{sr}$  is the mobility term due to surface roughness scattering. While phonon scattering has a strong temperature dependence, the other two mechanisms have a fairly weak dependence [9]. The mobility due to phonon scattering reduces with increase in temperature and hence dominates the effective mobility near room temperature in silicon inversion layers. However, unlike inversion mobilities in silicon, the inversion mobility of electrons in SiC has been reported to increase with temperature [8,10-12]. Exponential increase in conductivity with temperature has been reported in some papers [11,12] and explained as due to a thermally activated process.

The bulk electron mobility in SiC is anisotropic and varies significantly depending on the orientation [13]. In particular, the electron mobility in the c (0001) direction in 6H-SiC is 5 times lower than the mobility in the c plane. However, in 4H-SiC the electron mobility in the c direction is only 25% higher than in the c plane. Commercial SiC wafers typically have (0001) and (000 $\bar{1}$ ) faces and hence the lateral mobility of electrons that is measured in this work is in the c plane. Some electron mobility anisotropy is to be expected even in the c plane. The conductivity effective mass for 4H-SiC and 6H-SiC was calculated for different orientations using the values given in the M $\Gamma$  and MK directions (within the c plane) [14] assuming that the dispersion relation was ellipsoidal close to the minima and calculating the effective mass as follows:

$$m_{\theta} = \left( \prod_{n=1 \dots 6} \frac{1}{\frac{\cos(\theta - 60n)^2}{m_{M\Gamma}} + \frac{\sin(\theta - 60n)^2}{m_{MK}}} \right)^{1/6} \quad (2)$$

where  $\theta$  is the angle between the chosen orientation and the M $\Gamma$  direction. As expected, the effective mass was periodic with the orientation with a period of 60°. However, the peak-to-peak variation in the reciprocal effective mass (which is directly proportional to the mobility)

was only 1% in the case of 4H-SiC and about 3% in the case of 6H-SiC. The anisotropy is therefore quite small compared to the anisotropy between the c plane and the c direction. However, during off-axis growth, some steps are likely to form in the epitaxy and this may cause some in-plane anisotropy. It should be noted that in-plane anisotropy of inversion layer mobility has been observed in silicon [15].

Carrier mobilities in inversion layers are affected significantly by the effective normal electric semiconductor surface field applied from the gate [16]. The normal field also attracts the inversion layer carriers (in this case electrons) towards the interface where they may be subject to scattering by interface irregularities and asperities thus reducing the mobility. The effective semiconductor surface field by definition also varies directly as the inversion layer charge and thus variations in the inversion layer mobility as a function of the normal field will also include changes in the inversion mobility as a result of the inversion layer charge. A high normal field would result in a high inversion layer charge which would screen the carriers from other coulombic scattering centers. This screening would therefore tend to increase the mobility as the normal field increases contrary to the reduction in inversion layer mobility due to surface roughness scattering. While the coulombic scattering may be very small in modern silicon technology, it could be significant for SiC MOS devices and this screening could therefore have a significant effect.

### C. Device Fabrication

The devices were fabricated on aluminum doped 2 $\mu$ m thick P-type epitaxial layers with doping in the range  $(2.5-10 \times 10^{15} \text{ cm}^{-3})$  grown on the Si face of aluminum doped P-type substrates ( $3.5^\circ$  off-axis in the case of 6H-SiC and  $8^\circ$  off-axis in the case of 4H-SiC) with doping of about  $2 \times 10^{18} \text{ cm}^{-3}$ . The wafers were initially given a standard RCA clean without a subsequent HF dip. The wafers were then subjected to the following oxidation cycle: dry oxygen at  $1050^\circ\text{C}$  for 5 minutes, steam at  $1050^\circ\text{C}$  for 265 minutes and again in dry oxygen at  $1050^\circ\text{C}$  for 5 minutes. The 220 $\text{\AA}$  thick thermal oxide was removed by etching in dilute HF and the wafers were then cleaned using an RCA clean without a final HF dip. A low temperature oxide (LTO) of thickness about 7200 $\text{\AA}$  was deposited on the wafers as the field oxide and patterned to define the drain and source regions. The LTO deposition temperature was  $410^\circ\text{C}$  and the chamber pressure was 750 milliTorr during the deposition. The flow-rates were 150sccm of  $\text{O}_2$  and 75sccm of LTO-410 (di-ethyl silane). After etching the source-drain windows, a second LTO of thickness 1100 $\text{\AA}$  was deposited under identical conditions to act as the pad oxide during the subsequent high dose, high temperature, nitrogen implants ( $80\text{keV}:2 \times 10^{15} \text{ cm}^{-2}$ ,  $40\text{keV}:1 \times 10^{15} \text{ cm}^{-2}$  at  $1000^\circ\text{C}$ ) performed to create these drain-source regions. The gate oxide for these MOSFETs, which was about 850 $\text{\AA}$  thick and was deposited under identical conditions, underwent 5 principal thermal cycles as indicated in Table I. This



matrix enabled the separation of the effects of each critical cycle and allowed the evaluation of the need of each particular cycle

The first cycle is the thermal cycle used for the hot implant which perforce is used on all wafers. Split-1 is a duplication of the earlier process [8] which was used as a benchmark for the current process. However, the large wet oxidation time in this split would result in about 40Å of thermal oxide being grown under the deposited thinner gate oxide of the lateral MOSFETs. Since it is our conjecture that the deposited oxide resulted in high inversion layer mobilities due to reduced interface disorder and interface charges from aluminum incorporation, the thick thermal oxide could degrade the performance of the MOSFETs on this split. Therefore Split-2, which has reduced oxidation time at 1100°C, was designed to grow only 5Å of thermal oxide at the SiC interface. This is about the thickness of thermal oxide grown under the deposited field oxide in Split-1 in this process and during the previous run [8]. The effect of this interface thermalization was studied in Split-3 where the gate dielectric was subjected to only the 1100°C, 60 minute argon anneal and the 950°C, 60 minute re-oxidation anneal and not any oxidation at 1100°C. Since the field oxide in the previous process run [8] was subjected to the implant activation anneal in argon at 1250°C for 60 minutes, the

Table I. The Different Thermal Cycles Applied to the Different Splits

Device 1: Gate Oxide FET      Device 2: Field Oxide FET  
A = 1000C hot drain-source implant in argon for 60 minutes      B = Implant activation anneal at 1250C  
C = Wet nitrogen oxidation anneal for 400 minutes at 1100C      D = Wet nitrogen oxidation anneal for 60 minutes at 1100C  
E = In-situ argon anneal for 60 minutes at 1100C      F = 950C wet re-oxidation anneal in wet nitrogen for 60 minutes

All ramp-up in dry oxygen at 5C/min and inert ram-down at 3C/min

Split	Device	A	B	C	D	E	F
1	1	No	Yes	Yes	No	Yes	Yes
	2	Yes	Yes	Yes	No	Yes	Yes
2	1	No	Yes	No	Yes	Yes	Yes
	2	Yes	Yes	No	Yes	Yes	Yes
3	1	No	Yes	No	No	Yes	Yes
	2	Yes	Yes	No	No	Yes	Yes
4	1	No	No	No	Yes	Yes	Yes
	2	Yes	No	No	Yes	Yes	Yes



gate dielectric on the SiC pieces in these 3 splits were also subjected to this anneal. Subjecting the gate oxide to stressful thermal cycles is usually avoided during silicon MOSFET fabrication. However, since high mobilities were obtained on MOSFETs where the gate dielectric had been subjected to such a cycle in the previous run [8], the effect of this cycle was monitored using Split-4 which followed identical thermal cycles to Split-2 except that the gate dielectric in this split was not subjected to the implant activation cycle. After the fabrication of the gate dielectric, polysilicon was deposited using LPCVD at 550°C for 40 minutes and degenerately doped with phosphorus using phosphorus disks at 875°C. The gates were then patterned and aluminum ohmic contacts achieved to the gate, source and drain through a lift-off process followed by aluminum metallization on the backside of the wafer.

Different sets of MOSFETs were designed with W/L ratios:  $W/L = 160\mu\text{m}/5\mu\text{m}$ ,  $160\mu\text{m}/10\mu\text{m}$ ,  $160\mu\text{m}/20\mu\text{m}$ ,  $160\mu\text{m}/25\mu\text{m}$ ,  $160\mu\text{m}/40\mu\text{m}$ ,  $160\mu\text{m}/50\mu\text{m}$ , and  $160\mu\text{m}/80\mu\text{m}$ . By plotting the reciprocal of the on-resistance of the MOSFETs as a function of the W/L ratio, the mobility can be easily extracted from the slope of the straight line thus obtained. In this manner the parasitic resistances that may affect the on-resistance but would not be dependent on the W/L ratio could be accounted for, if the parasitic resistances are comparable or significant compared to the channel resistance. The parasitic resistances were expected to be negligible compared to the channel resistance for the longer MOSFETs (<3%). The (hexagonal close packing) HCP structure of SiC would tend to indicate some anisotropy in the inversion layer mobility measured either due to the differences in the effective masses of the electrons in the various directions or due to differences in the semiconductor surface roughness due to the off-axis epitaxial growth. To measure this anisotropy, MOSFETs of different W/L ratios were designed with the current flow at angles of 0°, 5°, 10°, 15°, 20°, 25°, 30°, 60°, and 90° to the wafer flat. MOS capacitors and gated-diodes were also incorporated into the layout.

#### D. Experimental Results

Capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were performed at room temperature on MOS capacitors situated near the MOSFETs, at frequencies from 1kHz to 1MHz using a HP 4284A precision LCR meter. The gate oxide capacitance was accurately determined using C-V measurements on capacitors of different gate areas. The effective oxide charge measured from the flatband voltage shifts on these capacitors was about  $2\text{-}5 \times 10^{11} \text{ cm}^{-2}$ . Output and transfer characteristics of the MOSFETs were measured using a Keithley Model 251 I-V system from room temperature up to 200°C. The output characteristics for typical lateral MOSFETs on 6H-SiC and 4H-SiC are shown in Figures 1 and 2 respectively. Excellent gate control is observed with well defined regions of linear dependence and current saturation. Transfer characteristics for typical MOSFETs on 4H-SiC and 6H-SiC are shown in Figures 3

and 4. The effective inversion mobility was extracted for gate biases in the range -5 to 50V from the transfer characteristics using:

$$\mu_{eff} = \left| \frac{I_D(V_{GS})}{C_{ox} \left( \frac{W}{L} \right) (V_{GS} - V_{Th}) V_{DS}} \right|_{V_{DS}=100mV} \quad (3)$$

where  $I_D(V_{GS})$  is the drain current at a gate bias of  $V_{GS}$ ,  $C_{ox}$  is the oxide capacitance,  $W$  is the channel width,  $L$  is the channel length,  $V_{Th}$  is the threshold voltage obtained by extrapolation of the tangent drawn to the characteristic at the point of maximum transconductance to the gate bias axis, and  $V_{DS}=100mV$  is the drain bias at which the characteristics are taken. The effective mobility was extracted for the longest MOSFETs fabricated with a  $W/L = (160\mu m/80\mu m)$  and the parasitic components of the resistance were found to be negligible ( $<3\%$ ) compared to the channel resistance. The effective mobility was extracted for MOSFETs with different orientations to the wafer flat, for different splits on the 2 polytypes at temperatures from  $25^\circ C$  to  $200^\circ C$  in steps of  $25^\circ C$  and plotted as a function of orientation with temperature as a parameter and as a function of the effective semiconductor surface field with temperature as a parameter.

#### E. Discussion

As was described previously, splits were designed into the process to allow the determination of the critical steps in the gate dielectric fabrication. The SiC pieces processed using Split-4 were found to have lower yield of about 50% with the main cause for failure

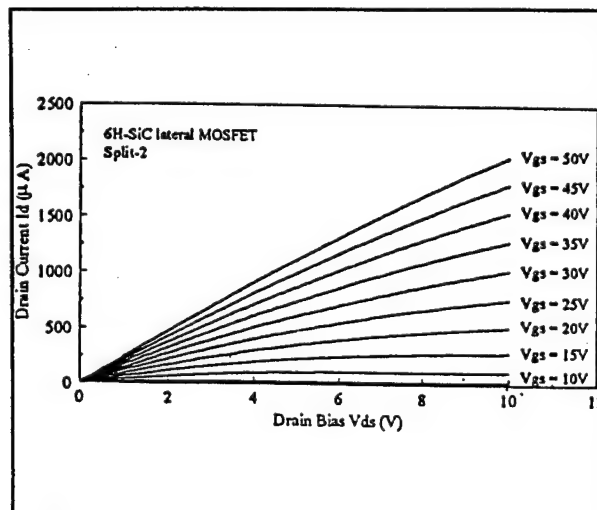


Figure 1. Output characteristics for lateral MOSFETs on 6H-SiC ( $W/L=160\mu m/80\mu m$ ) at room temperature up to a gate bias of 50V. Excellent gate control is observed.

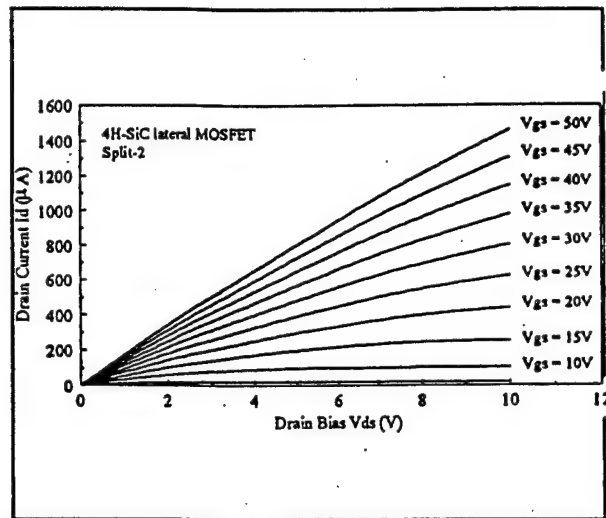


Figure 2. Output characteristics for lateral MOSFETs on 4H-SiC ( $W/L=160\mu\text{m}/80\mu\text{m}$ ) at room temperature up to a gate bias of 50V. Excellent gate control is observed.

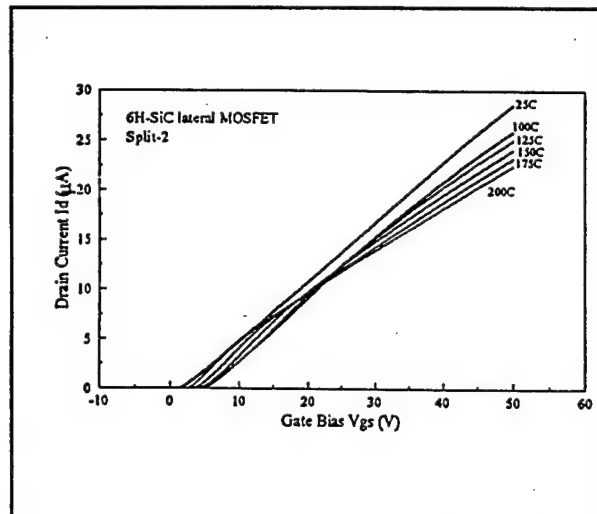


Figure 3. Transfer characteristics for lateral MOSFETs on 6H-SiC ( $W/L=160\mu\text{m}/80\mu\text{m}$ ) at room temperature up to a gate bias of 50V.

being gate-source shorts. Based upon this, we conclude that the high temperature of the implant activation anneal is required to improve the breakdown strength of the deposited oxide film. MOS capacitors and MOS-gated diodes on this split also showed the same tendency for gate-source shorts and high gate leakage current.

The SiC pieces processed using Split-3 had a high yield but had lower mobilities than Splits 1 and 2. This reduction was about 10% in the case of 6H-SiC and was about 20% in the case of 4H-SiC. Since the only difference between Split-3 and Split-2 is the fact that Split-2 underwent an additional 60 minute wet  $\text{N}_2$  anneal at  $1100^\circ\text{C}$ , the conclusion to be drawn is that

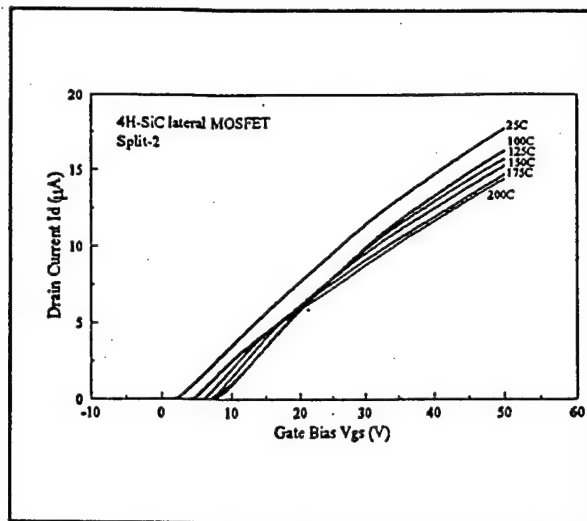


Figure 4. Transfer characteristics for lateral MOSFETs on 4H-SiC ( $W/L=160\mu\text{m}/80\mu\text{m}$ ) at room temperature up to a gate bias of 50V.

the thin layer of thermal oxide grown during this step and the additional thermalization of the deposited oxide is required to obtain higher mobilities in SiC lateral MOSFETs. It must however be pointed out that the mobilities measured in this split are still about  $63\text{ cm}^2/\text{V}\cdot\text{s}$  for 6H-SiC at room temperature which is comparable to the highest values reported on thermal oxide on 6H-SiC and about  $42\text{ cm}^2/\text{V}\cdot\text{s}$  for 4H-SiC at room temperature.

The 6H-SiC piece which underwent Split-1 suffered from poor contacts which were not improved even on reworking. Hence no data could be obtained from that piece. The 4H-SiC piece which underwent Split-1 however was satisfactory and an average inversion layer mobility of about  $52\text{ cm}^2/\text{V}\cdot\text{s}$  was measured on lateral MOSFETs on this piece at room temperature. Since this split was intended as the control split for comparison with data obtained on thick gate dielectric MOSFETs made in the previous run [8], the inversion layer mobility on the field oxide FETs on this piece were of special interest. Measurements on field oxide FETs on this piece also showed an inversion layer mobility of about  $50\text{ cm}^2/\text{V}\cdot\text{s}$  and a threshold voltage of about 26V. This indicates that the high inversion layer mobility can also be obtained on thin gate dielectric MOSFETs by using the LTO oxide process to form the gate oxide. Due to the fact that the best values of mobility were obtained on the devices in Split-2, it is these devices that are discussed in the following paragraphs.

The variation of the calculated effective mass of 6H-SiC and 4H-SiC with orientation is only about 2% as described previously. However, the steps in the SiC epitaxy which are perpendicular to the flat could also affect the mobility due to carrier scattering at those sites. As can be seen in the Figures 5 and 6, the difference between the inversion mobilities on the various orientations is not significant enough to allow us to determine any clear-cut orientation dependence in the mobility. The observed variation between the different orientations of about 5-10% is consistent with the theoretically calculated variation from one orientation to another of

only 2%. Thus, no obvious trends could be deduced regarding the orientation dependence since the differences were not significant.

The electric field dependence of inversion mobility is extremely useful in determining the dominant scattering mechanism. To study this dependence, the electric field dependence of the inversion mobility was studied with the temperature as a parameter. It can be seen from the Figures 7 and 8 that the electric field dependence is definitely affected by the temperature. At room temperature, the electric field dependence is weak and the mobility does not degrade much even at a normal field of 1 MV/cm especially for 6H-SiC. The field dependence at room temperature for 4H-SiC is slightly stronger.

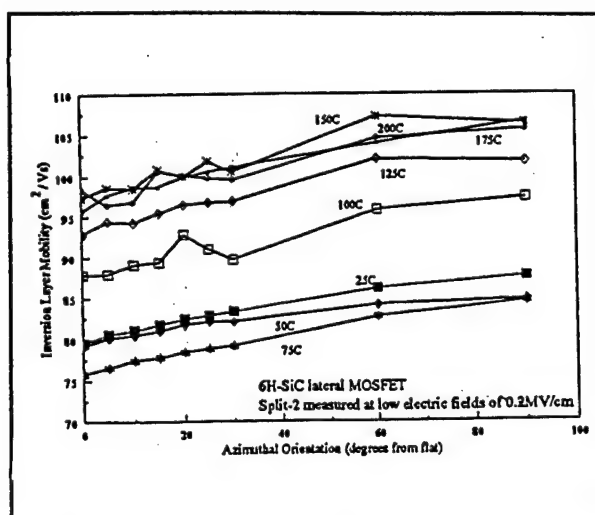


Figure 5. Plot of the inversion mobility in 6H-SiC as a function of device orientation at low electric fields with temperature as a parameter. The variation is only 5-10%.

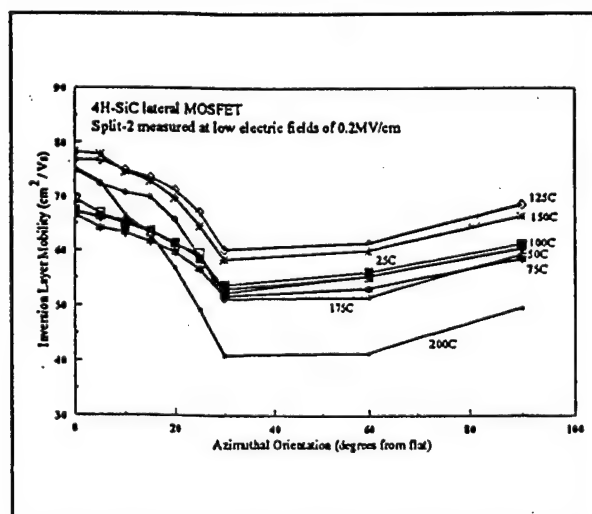


Figure 6. Plot of the inversion mobility in 4H-SiC as a function of device orientation at low electric fields with temperature as a parameter. The variation is only 5-10%.

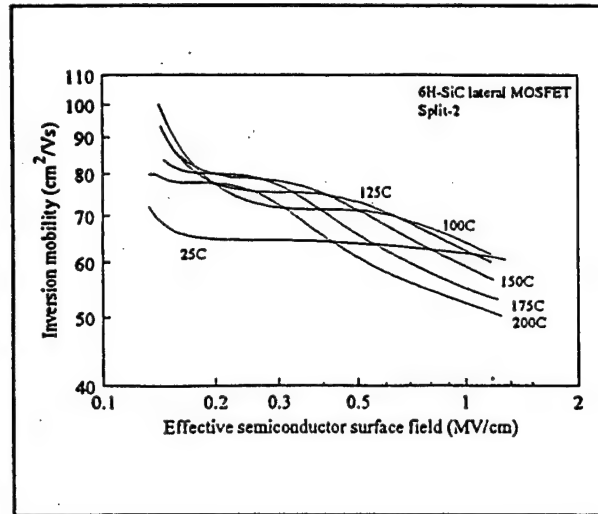


Figure 7. Plot of the inversion mobility in 6H-SiC as a function of the effective semiconductor surface field with temperature as a parameter. Note that at higher temperatures and higher fields, the dominant scattering mechanism is acoustic phonon scattering.

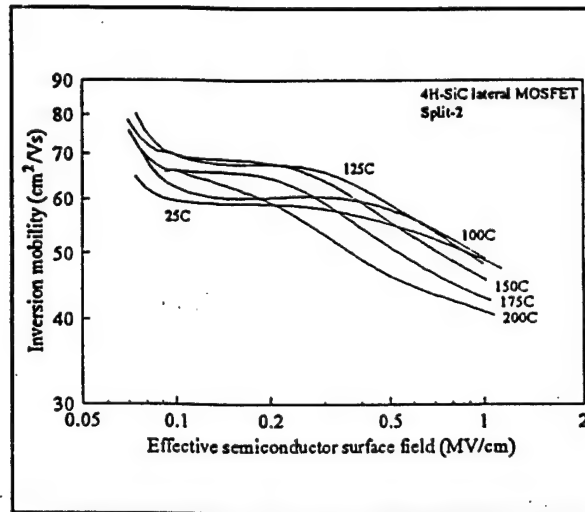


Figure 8. Plot of the inversion mobility in 6H-SiC as a function of the effective semiconductor surface field with temperature as a parameter. Note that at higher temperatures and higher fields, the dominant scattering mechanism is acoustic phonon scattering

The electric field dependence at higher temperatures ( $> 100^{\circ}\text{C}$ ) appears to be divided into 2 definite regimes. At lower fields, the electric field dependence is weak but as the field increases beyond a certain threshold, the field dependence increases. At the highest temperature measured ( $200^{\circ}\text{C}$ ), the electrons have a significant electric field dependence over the entire measured range. On a log-log plot of inversion layer mobility against the normal electric field, the dependence at higher fields for the higher temperatures was found to be linear. The electric field dependence in this regime was of the form  $E^{-\beta}$  where  $E$  is the normal field and  $\beta$  is

between 0.21 and 0.28. This dependence is close to the electric field dependence typically observed for acoustic phonon scattering in silicon inversion layers ( $\beta=0.3$ ) [15,17]. The fact that the intercepts of these straight line with the mobility axis reduce with temperature is again corroborative of a phenomenon such as acoustic phonon scattering. It should be pointed out that this electric field dependence was observed not only for different devices on the same die but also from split to split on the same polytype. The values also did not vary significantly from 6H-SiC to 4H-SiC. The typical electric field dependence due to surface roughness ( $\beta=2$ ) was not observed on these MOSFETs over this temperature and electric field range.

The temperature dependence of the inversion mobility is a very good indicator of the type of scattering mechanism that is dominant. In silicon MOSFETs at room temperature, acoustic phonon scattering is dominant at low fields and surface roughness scattering dominates at higher fields. However, in these SiC lateral MOSFETs, it is at higher temperatures and at higher fields that the dominant scattering mechanism observed is acoustic phonon scattering. At a high electric field and at temperatures in excess of 100°C, the dependence of the inversion mobility as a function of temperature at a particular electric field (in the range of 0.5-0.7 MV/cm) is of the form  $T^{-\alpha}$  where  $T$  is the temperature in Kelvin and  $\alpha$  is a constant in the range 0.81-1.13 for 6H-SiC and about 1.5 for 4H-SiC.

The theoretical temperature dependence of mobility in a two-dimensional electron gas due to surface acoustic phonons alone is  $T^{-1}$  [18] and the measured value of  $\alpha$  is in this range. The value of  $\alpha$  measured in inversion layers in silicon is around 1.5-1.75 [15,17]. The higher temperature dependence of inversion mobility in silicon is ascribed to phenomena other than surface acoustic phonon scattering such as scattering into other lower mobility valleys which require higher energy phonons as well as the presence of electrons in higher sub-bands due to the finite temperature [17].

It is worth pointing out that this paper provides the first report of a negative temperature dependence of inversion mobility in SiC indicating the dominance of phonon assisted scattering processes. Previous work on the temperature dependence of inversion mobility in SiC (6H-SiC) reported a thermally activated mobility due to an extremely disordered interface and a resultant large density of localized states in the conduction band tail [11,12]. This negative temperature dependence indicates that such a disorder is no longer the mobility limiting term when the gate dielectric is fabricated using the process described herein.

However, the above negative temperature dependence of inversion mobility is not observed in our devices at lower temperatures and at lower fields. In this regime, the inversion mobility is observed to increase with temperature as was observed previously in the literature [8,10,11,12]. In fact, at low fields of about 0.2 MV/cm, the inversion mobility increases with temperature from 25°C to about 125-150°C before decreasing with temperature at 175°C and 200°C. In conjunction with the weak electric field dependence in this regime, this suggests that



another scattering mechanism is dominant at low fields and at low temperatures with the acoustic phonon scattering becoming significant at the higher temperatures resulting in the negative temperature dependence at those temperatures.

The temperature dependence of this low field, low temperature scattering mechanism would tend to suggest some form of coulombic scattering. However, coulombic scattering is expected to have a definite positive dependence on electric field, or more accurately on the inversion charge which is proportional to the electric field, due to the screening effect of inversion charge on the ionized impurities and interface/oxide charges. Such a dependence was not observed even at the lowest temperature of 25°C. This could be due to the fact that at all temperatures and all fields measured, neither scattering mechanism is totally negligible. The effect of the acoustic phonon scattering could result in the slight negative electric field dependence of inversion mobility even at 25°C and the effect of the coulombic scattering could cause the electric field and temperature dependences in the high temperature and high field regimes to be slightly lower than the actual values. In summary, the measured inversion layer mobility at higher temperatures and higher fields can be described by the following equations:

$$\mu_{eff} = 2465 \left( \frac{T}{300} \right)^{-0.81} E_{eff}^{-0.25} \quad (4)$$

for 6H-SiC and,

$$\mu_{eff} = 4580 \left( \frac{T}{300} \right)^{-1.52} E_{eff}^{-0.28} \quad (5)$$

for 4H-SiC.

## F. Conclusions

Lateral MOSFETs were fabricated on both 6H-SiC and 4H-SiC using a LPCVD deposited and appropriately annealed oxide as the gate dielectric. Such MOSFETs with high inversion layer mobilities (110 cm<sup>2</sup>/V·s on 6H-SiC and 160 cm<sup>2</sup>/V·s on 4H-SiC) had been reported for the first time using a deposited annealed field oxide as gate dielectric [8]. The process was successfully repeated using LPCVD oxide of more conventional thickness to verify the principle that using an appropriately annealed deposited oxide instead of a thermal oxide can result in higher inversion mobilities in SiC. Inversion layer mobilities of 75 cm<sup>2</sup>/V·s on 6H-SiC and 55 cm<sup>2</sup>/V·s on 4H-SiC were measured at room temperature. This paper therefore confirms the basic principle of the previous work and confirms that deposited annealed gate dielectrics can be successfully used to obtain high inversion mobilities in SiC MOSFETs. We believe that phonon scattering limited inversion mobility has been measured at higher temperatures and fields for the first time in SiC inversion layers.

## G. Acknowledgements

The authors would like to thank the sponsors of the Power Semiconductor Research Center and ARPA for supporting this work.

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### III. Role of Defects in Producing Negative Temperature Dependence of Breakdown Voltage in SiC

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Electron beam induced current (EBIC) techniques were employed in order to understand the role of defects on the breakdown characteristics of SiC. EBIC images revealed that certain defects caused enhanced multiplication leading to the catastrophic failures in SiC diodes. The impact ionization coefficients for holes measured at the defective site ( $\alpha_{p,eff}$ ) were found to be higher than those measured at a non-defective site. Also,  $\alpha_{p,eff}$  measured at the defective site was found to increase with increasing temperature in contrast with a defect free diode where  $\alpha_p$  decreases with increasing temperature, clearly indicating that the defects produce the observed negative temperature coefficient of breakdown voltage in SiC.

#### A. Introduction

One of the most important parameters of power device is its breakdown voltage. It is important that the breakdown voltage of a device increase with temperature for it to have stable reliable behavior. This behavior requires a decrease in impact ionization coefficients ( $\alpha$ ) with increasing temperature. Although a decrease in impact ionization coefficients for holes ( $\alpha_p$ ) have been reported with temperature in a defect free diode for both 6H and 4H-SiC [1], there have been contradictory reports in the literature on the variation of breakdown voltage with temperature. Earlier reports by Palmour *et al.* [2], Kimoto *et al.* [3], and Raghunathan *et al.* [4] indicated negative temperature coefficient for breakdown in SiC. However, recent publications by Neudeck *et al.* [5] and Mitlehner *et al.* [6] indicate positive temperature coefficients for breakdown in SiC. In this paper, we report evidence of defects causing a negative temperature coefficient of breakdown voltage in SiC for the first time.

#### B. Experimental Procedure

In our measurements, the electron beam induced current (EBIC) technique was used in a Scanning electron microscope (SEM) to first identify the location of electrically active defects. An experimental setup was established using EBIC [7] that allows us to apply reverse biases as high as 1000 V on these diodes to image sites of enhanced multiplication. The SEM also has a specially designed heating stage that allows us to perform EBIC studies on the same diodes at various temperatures. After isolating defects causing enhanced multiplication, impact ionization measurements were performed at these defective sites at different temperatures, using a pulsed-EBIC setup described in an earlier publication [1].

Schottky barrier diodes were fabricated on P-type 6H and 4H-SiC ( $5 \times 10^{15} \text{ cm}^{-3}$ ,  $2 \text{ }\mu\text{m}$  thick) homoepitaxial layers grown on off-axis SiC substrates ( $3 \times 10^{18} \text{ cm}^{-3}$ ). Prior to metal deposition, the SiC wafer was given a Huang clean. Schottky diodes ( $60\text{-}200 \text{ }\mu\text{m}$  diameter) were fabricated using a shadow mask with sequential evaporation of Ti ( $2000 \text{ }\text{\AA}$ ) and Al ( $2000 \text{ }\text{\AA}$ ) layers. Blanket evaporation of a Ti/Al layer was also done on the heavily doped substrate to form a large area backside contact. An argon implant was performed around the edges to obtain nearly ideal breakdown [8].

### C. Results and Discussion

The breakdown characteristics of 6H and 4H-SiC diodes studied using reverse I-V measurements, indicated negative temperature coefficient of breakdown voltage, the details of which are reported in ref. [9]. Fig. 1a shows an EBIC image of an argon ion implant terminated 4H-SiC diode at a reverse bias of  $150 \text{ V}$ . The bright spot at the center indicates enhanced multiplication at a defective site in the diode. This diode catastrophically failed at this defective site at a bias of  $200 \text{ V}$  leaving a crater as shown in Fig. 3b. Although, the nature of the defects is not known, the high multiplication at the defective site could be due to various reasons: (a) If a defect is located in the depletion region it may act to locally enhance the electric field in that region leading to enhanced multiplication; (b) There could be distortions in the band structure caused by lattice strain at the defective site which would lead to enhanced multiplication for the same electric field values; (c) There could be a crystal growth imperfection causing a different polytype to be grown in that region leading to higher impact  $\alpha$  values at the defective site; (d) There could be impurities with many states in the bandgap that aid in transporting the carriers from the valence band to the conduction band during impact ionization. Hence, we coin the term effective impact ionization coefficients for holes ( $\alpha_{p,\text{eff}}$ ) to define  $\alpha$  values measured at the defective site. As we can see from Fig. 2,  $\alpha_{p,\text{eff}}$  at this defective site is much higher than  $\alpha_p$  measured at a non-defective site. The enhanced multiplication at the defective site leads to the catastrophic failure seen in Fig. 1b.

In order to study the role of defects on the temperature coefficient of breakdown voltage in SiC, EBIC studies were performed on 6H-SiC diodes at various temperature. Fig. 3a is an EBIC image of an unterminated 6H-SiC diode at room temperature and at a reverse bias of  $250 \text{ V}$ . As we can see in this image, there is enhanced EBIC signal at the edges because of the high electric fields. However, there is no clear indication of enhanced multiplication at any defective site. In contrast, on heating the diode to  $150^\circ\text{C}$ , we clearly observed a bright spot at the edge of the diode at the same reverse bias of  $250 \text{ V}$ , indicating enhanced multiplication at a defective site as shown in Fig. 3b. Impact ionization measurements were performed at the defective site both at room temperature and at  $150^\circ\text{C}$ . As shown in Fig. 2,  $\alpha_{p,\text{eff}}$  increased with temperature at the defective site, in contrast to a decrease in  $\alpha_p$  measured at a non-defective site.

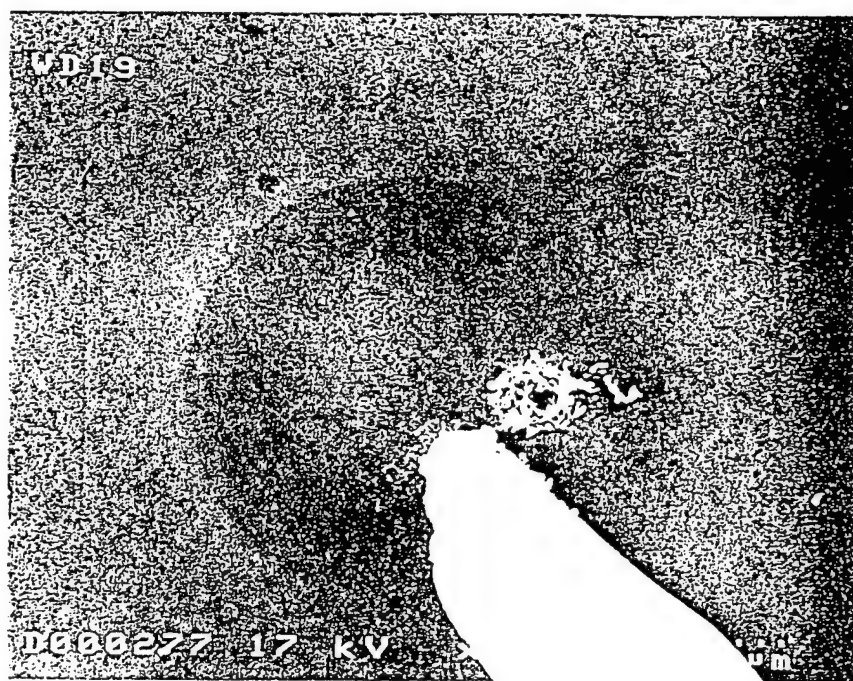


Figure 1. (a) EBIC Image of a 4H-SiC Schottky diode at a reverse bias of 150 V at room temperature; (b) diode after catastrophic failure at 200 V at the same defective site.

This provides the first definitive and conclusive evidence that defects are responsible for the previously reported decrease in breakdown voltage with increasing temperature in silicon carbide devices.

#### D. Conclusions

This paper provides the first conclusive evidence that defects are responsible for the observed decrease in breakdown voltage in SiC diodes. Impact ionization coefficients measured at room temperature at the defective site have been found to be higher than at a non defective site as a result of which breakdown occurs at the defect site before the ideal breakdown voltage can be reached. Further,  $\alpha_p$  in a defect free site has been found to decrease with increasing temperature while  $\alpha_{p,eff}$  at the defective site increases with increasing temperature. This provides proof that the defects are responsible for the observed negative temperature coefficient of breakdown voltage previously reported for SiC devices. Enhanced

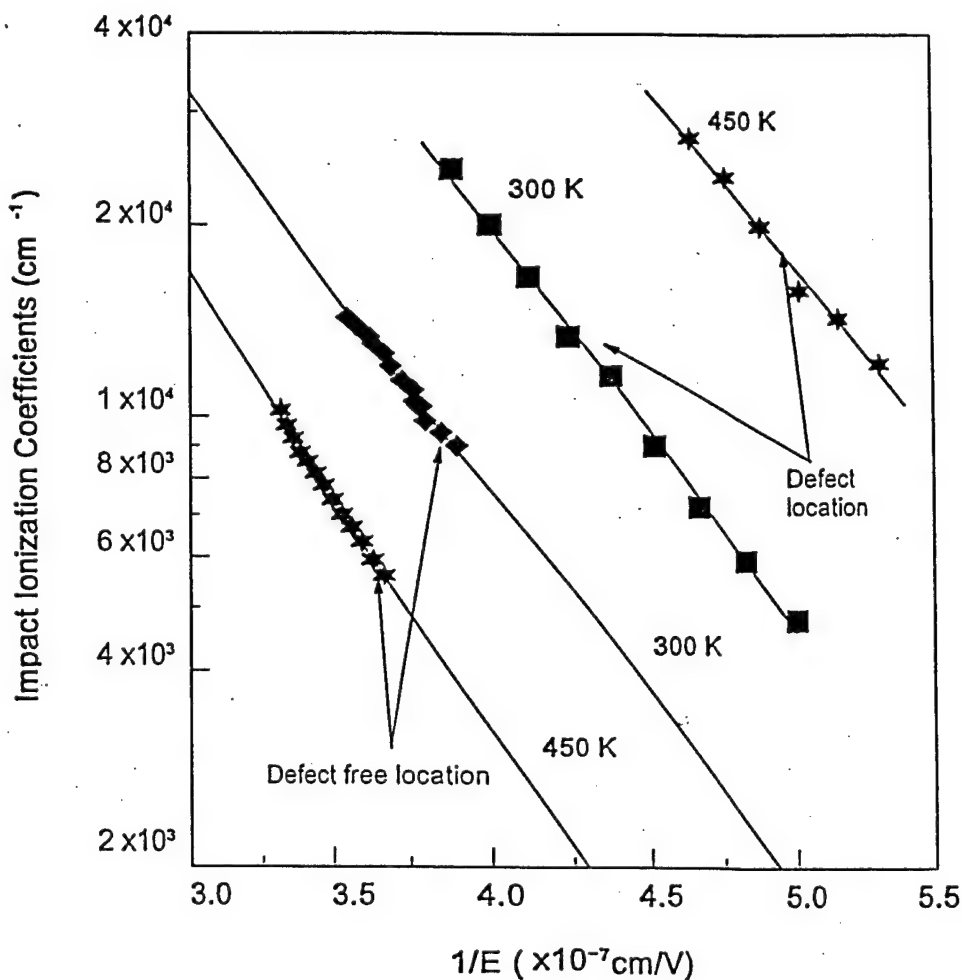


Figure 2. Impact ionization coefficients measured at a defective site ( $\alpha_{p,eff}$ ) compared to those measured at a non-defective diode ( $\alpha_p$ ) at room temperature and at 150°C in 6H-SiC.



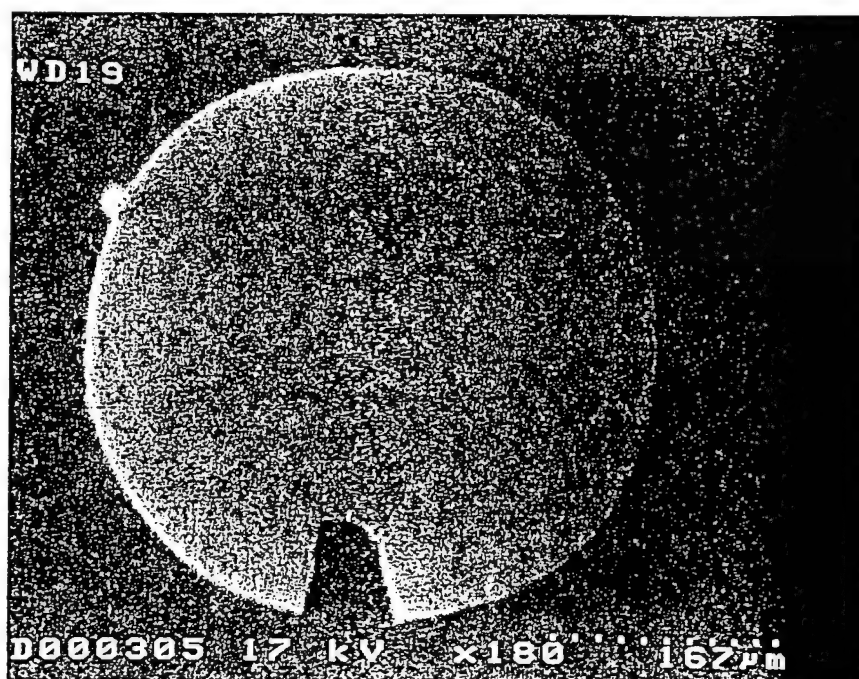
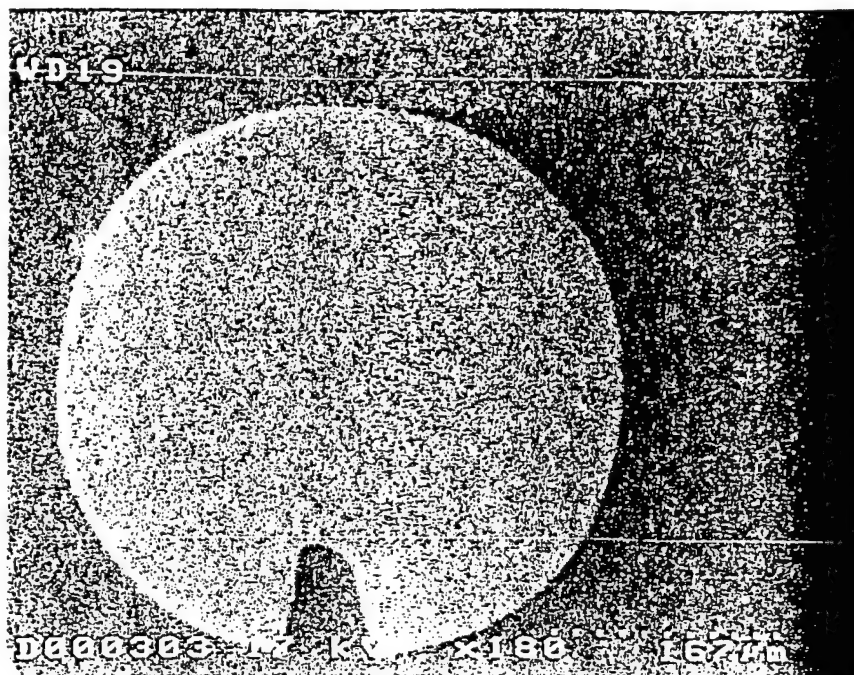


Figure 3. (a) EBIC image of a 6H-SiC diode at room temperature at a reverse bias of 250 V; (b) EBIC image of the same diode at 150°C at a reverse bias of 250 V.



multiplication at the defect has been shown to lead to catastrophic failure at the defective sites. From our results, it can be concluded that SiC devices, with the desired positive temperature coefficient for breakdown essential for stable operation, can be fabricated if the defects can be eliminated.

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#### IV. Temperature Dependence of Hole Impact Ionization Coefficients in 4H and 6H-SiC

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Hole impact ionization coefficients have been accurately measured as a function of temperature in both 4H and 6H-SiC using the pulsed electron beam induced current (PEBIC) technique. For Chynoweth's equation ( $\alpha = a e^{-b/E}$ ), our measurements gave an  $a_p$  value of  $(2.5 \pm 0.2) \times 10^6/\text{cm}$  and a  $b_p$  value of  $(1.5 \pm 0.2) \times 10^7 \text{ V/cm}$  for 6H-SiC at room temperature while the values of  $a_p$  and  $b_p$  for 4H-SiC were found to be  $(3.5 \pm 0.4) \times 10^6/\text{cm}$  and  $(1.8 \pm 0.4) \times 10^7 \text{ V/cm}$ , respectively, at room temperature. An analytical solution to the variation of the ionization coefficients as a function of the electric field of the form  $\alpha = mE^n$  was derived in 6H and 4H-SiC, which will allow us to obtain close-form solutions for avalanche breakdown voltage for abrupt junctions with the same values as that obtained using the Chynoweth's Equation. The coefficient  $a_p$  was found to decrease with increasing temperature for both polytypes while the coefficient  $b_p$  remained constant. Based upon this data, the breakdown voltage of the 4H and 6H-SiC devices is predicted to increase with temperature which is an important desirable characteristic for power devices.

##### A. Introduction

Silicon carbide has received increasing attention for power switching, microwave and high temperature applications due to its high breakdown electric field, thermal conductivity and electron saturation drift velocity. One of the most important parameters of a SiC power device is its breakdown voltage. In order to obtain a clear understanding of its breakdown characteristics, it is important to have an exact knowledge of the impact ionization coefficients for SiC. It is also important that the breakdown voltage of a device increase with temperature for it to have stable reliable behavior. This behavior requires a decrease in impact ionization coefficients with increasing temperature. The impact ionization coefficients not only determine the reverse characteristics of a device but also influence the on-state voltage drop of a power MOSFETs and Schottky rectifiers [1] because the specific on-resistance of the drift region is given by:

$$R_{on,sp(ideal)} = \frac{4BV^2}{\epsilon_s \mu E_c^3} \quad (1)$$

where BV is the breakdown voltage,  $\epsilon_s$  is the dielectric constant,  $\mu$  is the carrier mobility, and  $E_c$  is the critical electric field for breakdown. The denominator ( $\epsilon_s \mu E_c^3$ ) has been referred to as Baliga's Figure of Merit (BFOM) [2] and used to compare the relative performances of various semiconductor materials for power device applications. Since the critical electric field for breakdown ( $E_c$ ) is dependent on the impact ionization coefficients [3], the specific on-resistance becomes strongly dependent on the impact ionization coefficients of the material. Hence, it is important to have accurate values of the impact ionization coefficients and its variation with temperature to assess the performance of any semiconductor material for power device applications.

However, there is very little information available in literature for 6H-SiC [4-5] and 4H-SiC [6] and more so on its variation with temperature [7]. Also, there have been contradictory reports in the literature on the variation of breakdown voltage with temperature. Earlier reports by Palmour *et al.* [8] and Kimoto *et al.* [9] indicated negative temperature coefficient for breakdown in SiC. However, recent publications by Neudeck *et al.* [10] and Mitlehner *et al.* [11] indicate positive temperature coefficients for breakdown in SiC. The variation of breakdown voltage with temperature can be conclusively obtained if we have information on the variation of impact ionization coefficients with temperature. In this paper, the impact ionization coefficients for holes are reported for 4H and 6H-SiC as a function of temperature using measurements by the pulsed electron beam technique. It is demonstrated that the data obtained from these measurements allows a more accurate simulation of reverse breakdown voltage characteristics than that obtained using previously published data. It is established from these measurements that the breakdown voltage of both 4H and 6H-SiC should increase with increasing temperature as has been observed in silicon. These results have widespread utility for SiC device analysis and design.

## B. Measurement Methodology

The method used in this work for measurement of impact ionization coefficients ( $\alpha$ ) is based on the pulsed electron beam induced current (P-EBIC) technique described in detail in an earlier report [12]. Carriers are generated in the depletion region of a reverse biased diode by a pulsed electron beam. At sufficiently high reverse biases, these carriers undergo multiplication due to impact ionization in the depletion region. The generated current is tracked in using a lock-in-amplifier and a plot of the generated current as a function of reverse bias is thus obtained. From this plot, impact ionization coefficients can be extracted using the following analytical solution [12].

$$\alpha_p = \frac{\ln(M_p)}{W} \quad (2)$$

Where  $\alpha_p$  is the impact ionization coefficients for holes,  $M_p$  is the holes multiplication factor, and  $W$  is the epilayer thickness. The validity of this extraction technique for a constant field profile has been verified by simulations as discussed in detail in an earlier report [12].

There are many important issues that need to be considered to obtain accurate measurement of  $\alpha$ : (a) Electric field crowding at the edges of diodes leads to errors if the measurement is made at a site including the edge. To eliminate such errors, measurements were made at a localized spot at the center of the diode by using a local generation area created with a stationary focused electron beam. (b) Electric field crowding at the diode edges also results in reducing the breakdown voltage to below the parallel plane case. This can reduce the maximum achievable multiplication at the center of the diode, thus limiting data extraction. To avoid this problem in our work, a Schottky diode structure with argon ion implant edge termination [13] was used to obtain nearly ideal breakdown voltage. (c) Defects are known to severely affect the breakdown characteristics of devices. Since the defect density of commercially available SiC wafers is known to be in the order of  $10^4 \text{ cm}^{-2}$  [14], devices were fabricated with area of less than  $5 \times 10^{-5} \text{ cm}^2$  so that at least half of the diodes were free of dislocations and micropipes. (d) In order to obtain data representing bulk SiC, it is important to perform measurements at a defect free site. In our measurements, the electron beam induced current (EBIC) technique was used to first identify the location of electrically active defects. An experimental setup was established using EBIC [15] that allows us to apply high reverse biases on these diodes and image sites of enhanced multiplication in the diodes. Thus, it was possible to choose a defect free region for the  $\alpha$  measurements allowing us to obtain accurate data for the extraction of impact ionization coefficients.

Previous measurements of impact ionization reported in SiC have all been made using the photo-multiplication technique [4-8]. There are various limitations to this technique. Since the beam size of the light pulse is large ( $\sim 50\text{--}100 \text{ }\mu\text{m}$ ), there is a high probability that there are defects at the measurement site which could lead to errors in the measured data. Secondly, since the device size has to be larger than the beam size (to avoid edge field effects), it is not possible to fabricate devices that are small enough to be defect free diodes. Since high multiplication cannot be attained in a defective diode, it is difficult to obtain sufficient data points for the accurate extraction of the ionization coefficients. Finally, with the use of an electron beam, it is possible to image the electrically active defects in the device and hence perform the measurement in a defect free site. However, this cannot be done using an optical beam method. Hence, we believe that the technique adopted in our work leads to a more accurate measurement of the impact ionization coefficients than reported in the literature [5-7].

### C. Measurement Setup

A schematic of the impact ionization measurement setup is shown in Fig. 1. A scanning electron microscope (Hitachi S-2700) was used for the generation of carriers using the electron beam. The electron beam was pulsed using a beam blanking setup in conjunction with the scanning electron microscope. The beam blanking device essentially consists of two electrodes, placed in the electron gun region, which are used to deflect the beam with an externally applied bias. The external bias is a pulse produced by a pulse generator which is also input into the lock-in amplifier as a reference. The photocurrent generated by the pulsed electron beam excitation of the reverse biased Schottky diode is tracked using the lock-in amplifier. This current is then plotted as a function of the applied reverse bias voltage (measured using a digital multimeter) across the Schottky diode. A curve of the multiplication versus electric field is then obtained from this data, from which impact ionization coefficients are extracted. The use of a sample heater within the SEM made it feasible to perform measurements up to temperatures as high as 500 K allowing us to obtain  $\alpha$  as a function of temperature. The entire setup was automated using a graphical programming tool called LABVIEW to allow us to perform extensive measurements with accurate data acquisition.

### D. Device Fabrication and Characterization

Schottky barrier diodes were fabricated on P-type 6H and 4H-SiC ( $5 \times 10^{15} \text{ cm}^{-3}$ ,  $2 \mu\text{m}$  thick) homoepitaxial layers grown on off-axis SiC substrates ( $3 \times 10^{18} \text{ cm}^{-3}$ ). Prior to metal

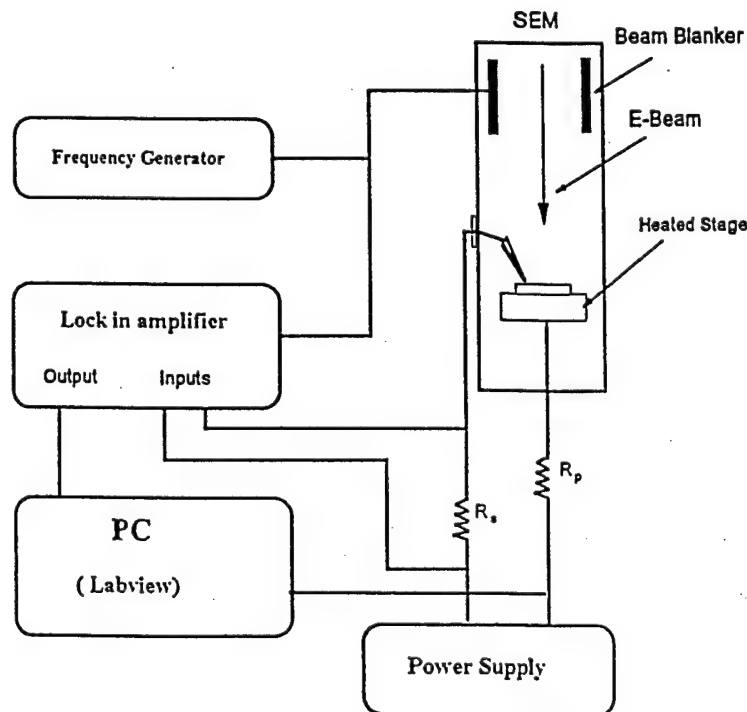


Figure 1. Schematic of the P-EBIC experimental setup.

deposition, the SiC wafer was given a Huang clean. Schottky diodes (60-100  $\mu\text{m}$  diameter) were fabricated using a shadow mask with sequential evaporation of Ti (2000 Å) and Al (2000 Å) layers. Blanket evaporation of a Ti/Al layer was also done on the heavily doped substrate to form a large area backside contact. An argon implant was performed around the edges to obtain nearly ideal breakdown [13]. The exact doping concentration and thickness of the epitaxial layers was obtained using C-V measurement. From the C-V measurements, the average doping concentration in the drift region was determined to be  $(6\pm1)\times10^{15} \text{ cm}^{-3}$  for 6H-SiC and  $(1\pm0.5)\times10^{16} \text{ cm}^{-3}$  for 4H-SiC. The thickness of the epitaxial layer was found to be 1.6  $\mu\text{m}$  for 6H-SiC and 2  $\mu\text{m}$  for 4H-SiC. As we can see from Eq. (2), the extraction of  $\alpha_p$  critically depends on the epilayer thickness which varies across the wafer. Hence CV measurements were made at every measurement site before calculating the impact ionization coefficients. The forward and reverse characteristics of the diode was studied using I-V measurements. The P-type 6H and 4H-SiC were found to exhibit breakdown voltages of 530 V and 570 V, respectively, with leakage currents as low as  $10^{-5} \text{ A/cm}^2$  at a reverse bias of 400 V [16].

#### E. Impact Ionization Data

Typical plots of multiplication factor  $M$  as a function of the reverse bias for both 6H and 4H-SiC [12] obtained using the setup described above are shown in Fig. 2 for diodes operating at room temperature. It can be seen from these plots that our procedure allows measurements to be performed up to relatively large values of multiplication factor ( $M$ ). Using this data, the impact ionization coefficients for holes in 6H-SiC and 4H-SiC could be obtained as a function of the electric field ( $E$ ) over a broad range. The measured data for 6H-SiC is compared with the values generally used for simulations [4] in Fig. 3. Our measured values were found to be lower than the commonly used values reported earlier. This indicates that a higher breakdown voltage is achievable in SiC devices for any given doping concentration than that calculated in earlier publications. Using the automated setup, extensive measurements of impact ionization coefficients were performed on many diodes across the wafer.  $\alpha_p$  was found to vary as a function of the electric field as dictated by the Chynoweth's law [17]:

$$\alpha = a e^{\frac{-b}{E}} \quad (3)$$

The variation of  $a_p$  and  $b_p$  across the wafer is summarized in Table I for both 4H and 6H-SiC. As seen in Table I, from our measurements,  $a_p$  in 6H-SiC has a value of  $(2.5\pm0.2)\times10^6 / \text{cm}$  and  $b_p$  has a value of  $(1.5\pm0.2)\times10^7 \text{ V/cm}$  at room temperature while  $a_p$  in 4H-SiC has a value of  $(3.3\pm0.4)\times10^6 / \text{cm}$  and  $b_p$  has a value of  $(1.77\pm0.4)\times10^7 \text{ V/cm}$  at room temperature.

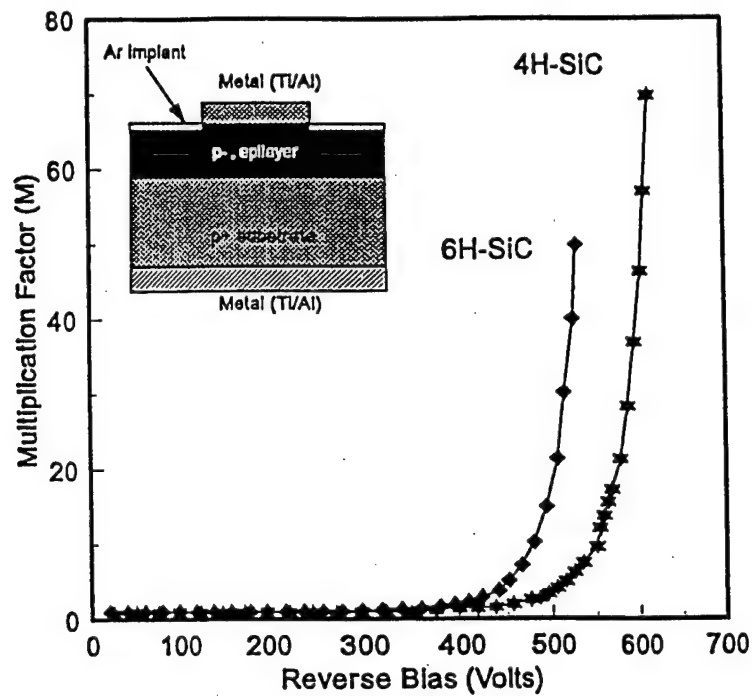


Figure 2. Measured multiplication factor as a function of the reverse bias on Schottky diodes for 4H and 6H-SiC. The inset shows the device structure used for the measurements.

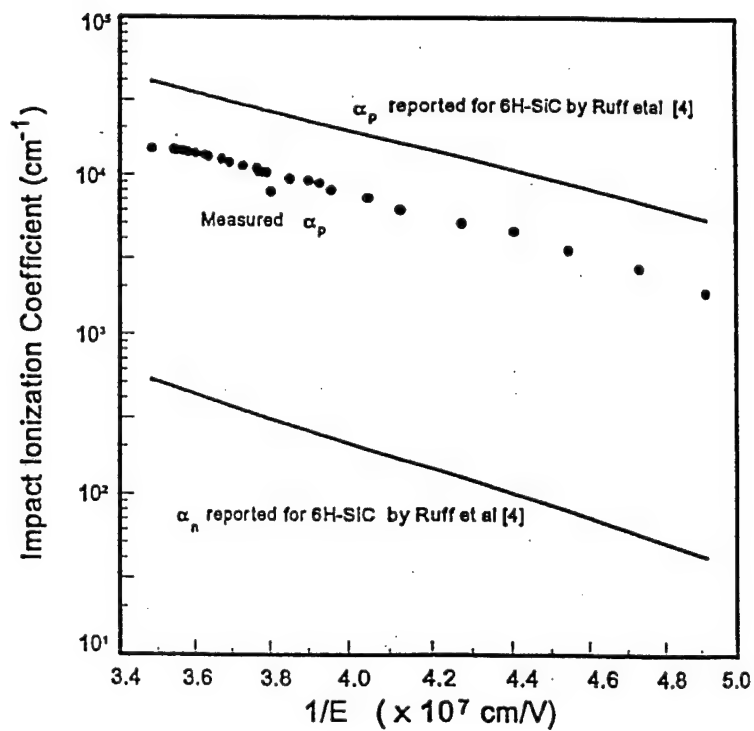


Figure 3. Measured impact ionization coefficients for holes in 6H-SiC compared with the values reported in the literature.



Table I. Impact Ionization Coefficient Parameters Measured Across the Wafers on 4H and 6H-SiC

No	Material	$a_p$ ( /cm )	$b_p$ ( V/cm )
1.	6H-SiC	$2.3 \times 10^6$	$1.52 \times 10^7$
2.	6H-SiC	$2.5 \times 10^6$	$1.49 \times 10^7$
3.	6H-SiC	$2.7 \times 10^6$	$1.49 \times 10^7$
4.	6H-SiC	$2.6 \times 10^6$	$1.51 \times 10^7$
5.	6H-SiC	$2.6 \times 10^6$	$1.49 \times 10^7$
6.	6H-SiC	$2.5 \times 10^6$	$1.49 \times 10^7$
7.	6H-SiC	$2.7 \times 10^6$	$1.50 \times 10^7$
8.	6H-SiC	$2.6 \times 10^6$	$1.49 \times 10^7$
9.	6H-SiC	$2.6 \times 10^6$	$1.49 \times 10^7$
10.	4H-SiC	$3.6 \times 10^6$	$1.74 \times 10^7$
11.	4H-SiC	$3.5 \times 10^6$	$1.73 \times 10^7$
12.	4H-SiC	$2.9 \times 10^6$	$1.64 \times 10^7$
13.	4H-SiC	$3.1 \times 10^6$	$1.69 \times 10^7$
14.	4H-SiC	$3.7 \times 10^6$	$1.77 \times 10^7$
15.	4H-SiC	$3.2 \times 10^6$	$1.70 \times 10^7$
16.	4H-SiC	$3.0 \times 10^6$	$1.69 \times 10^7$
17.	4H-SiC	$3.2 \times 10^6$	$1.71 \times 10^7$

Variation of impact ionization coefficients was measured as a function of temperature for both 6H-SiC and 4H-SiC by using the heating stage inside the SEM upto temperatures as high as 500 K. Typical data are shown in Fig. 4 and Fig. 5 for 6H-SiC and 4H-SiC, respectively. The observed negative temperature coefficient for  $\alpha_p$  implies an increase in breakdown voltage with temperature for both 4H and 6H-SiC. This is an important desirable characteristic as this ensures stable reliable behavior of power devices. The coefficients  $a_p$  and  $b_p$  calculated at each temperature for 4H and 6H-SiC from the data in Fig. 4 and Fig. 5 are plotted in Fig. 6 and Fig. 7, respectively. It can be seen that the coefficient  $b_p$  remains fairly constant with temperature, while the coefficient  $a_p$  varies linearly with temperature for both 4H and 6H-SiC as given below:

$$\text{In 6H-SiC :} \quad a_p = 4.6 \times 10^6 - 7.4 \times 10^3 T \quad (T \text{ in Kelvin}) \quad (4)$$

$$\text{In 4H-SiC :} \quad a_p = 6.3 \times 10^6 - 1.07 \times 10^4 T \quad (T \text{ in Kelvin}) \quad (5)$$

These expressions can be utilized for device simulation and analysis.

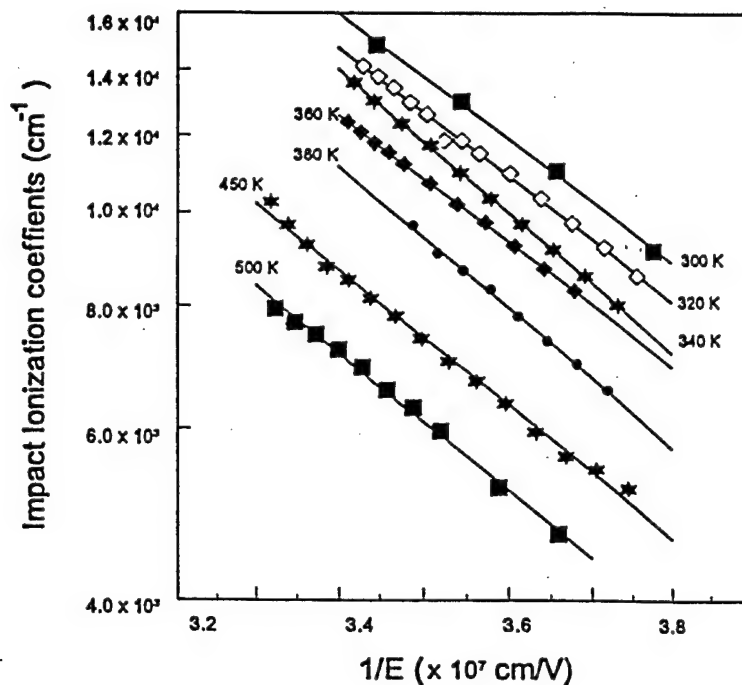


Figure 4. Measured hole impact ionization coefficients for 6H-SiC at temperatures ranging from 300 K to 500 K.

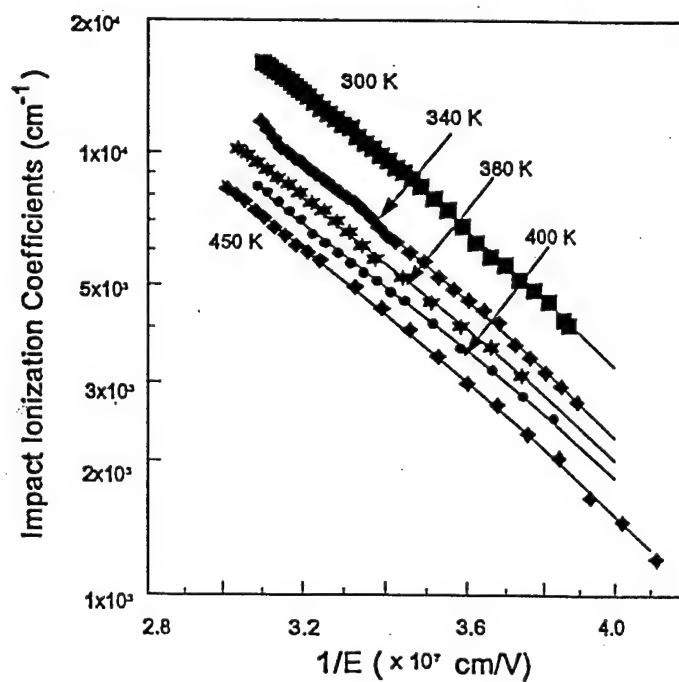


Figure 5. Measured hole impact ionization coefficients for 4H-SiC at temperatures ranging from 300 K to 500 K.

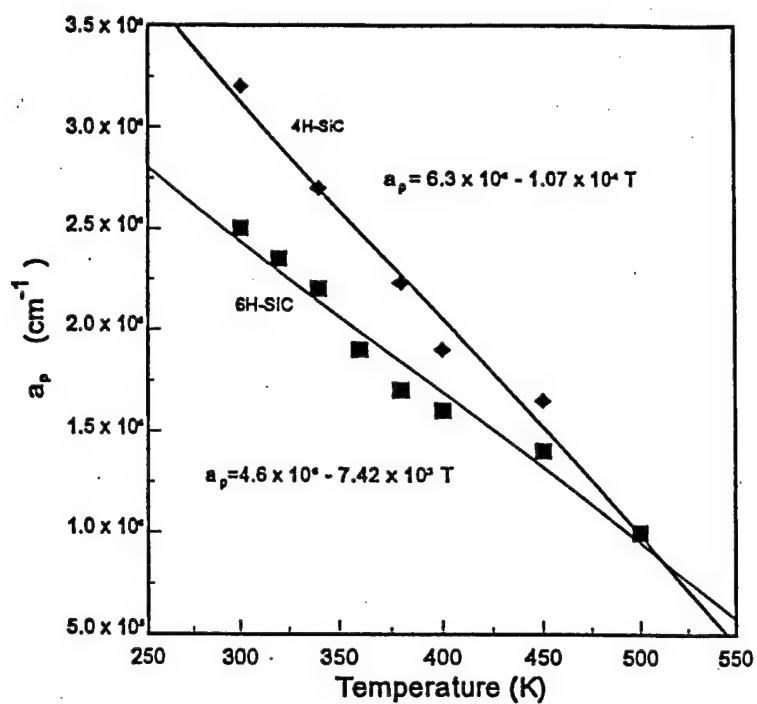


Figure 6. Temperature dependence of the coefficient  $a_p$  for 4H and 6H-SiC.

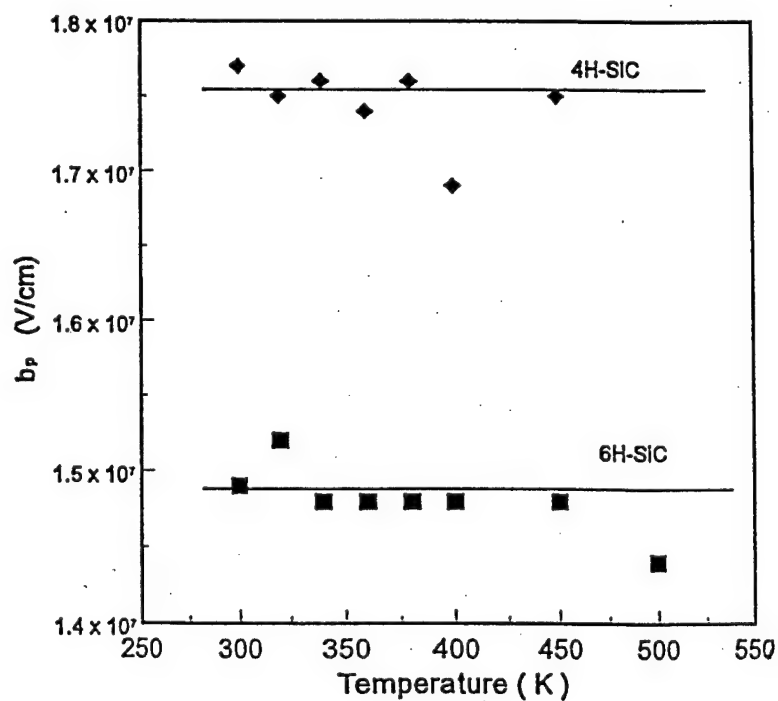


Figure 7. Temperature dependence of the coefficient  $b_p$  for 4H and 6H-SiC.

## F. Discussion

A comparison of values reported by Konstantinov *et al.* [6] to our measured data in 4H-SiC can be made by using Fig. 8. It can be seen that our measurements indicate much lower values for  $\alpha_p$  in 4H-SiC than the values measured by Konstantinov *et al.* [6]. We believe that our measurements are more accurate for the following reasons. The authors [6] have calculated ionization coefficients using the photo-multiplication current measured in the dc mode. We have used a pulsed electron beam for carrier generation and the advantages of using an electron beam source over an optical beam source has been substantiated earlier. Secondly, in the dc mode, it is very difficult to separate out the contributions of the leakage current and the generation current in the collected signal, particularly close to breakdown where the leakage increases substantially. However, in our measurements, we use a lock-in-amplifier that eliminates the dc leakage current and only measures the generated ac signal. Also, the authors [6] have used the observation of bright spots of light emission to eliminate bad diodes. This technique, although simple, is not as accurate in determining the defective regions as the EBIC technique used in our measurements. Finally, the authors [6] have obtained impact ionization coefficients using a curve-fitting technique to the measured multiplication versus reverse bias plot. The assumption used by the authors in order to curve fit the data (i.e.  $\alpha_n/\alpha_p = \text{a constant } K$ ) is not valid for all electric field values. In contrast, in our technique we have used a direct measurement of  $\alpha_p$  in SiC and these measurements clearly indicate that  $\alpha_p$  varies as given by

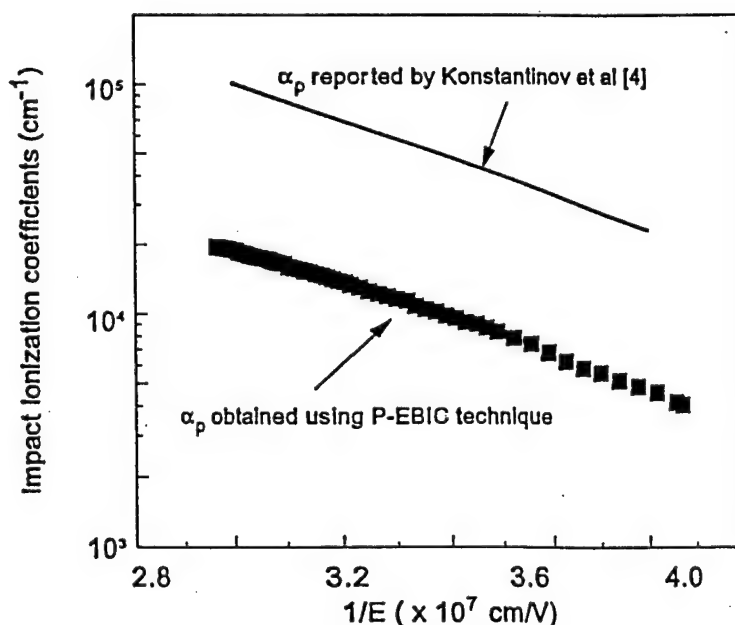


Figure 8.  $\alpha_p$  measured in 4H-SiC using our P-EBIC technique is much lower than the values reported by A. O. Konstantinov *et al.* [4].

the Chynoweth equation. As a final corroboration of our extracted values, we have shown earlier [12] that simulations performed using the measured coefficients (a and b) gave a breakdown voltage of 520 V in 6H-SiC which is the same as the experimentally observed data for 6H-SiC. In comparison, the simulated breakdown voltage obtained using data in ref. [6] was only 450 V.

In order to obtain closed-form solutions for the avalanche breakdown voltage in SiC, it is useful to use a power law for the variation of the impact ionization coefficients with electric field similar to that suggested by Fulop [18] for silicon. We suggest the following equations for silicon carbide:

$$\text{6H-SiC:} \quad \alpha = 6.6 \times 10^{-36} E^6 \quad (6)$$

$$\text{4H-SiC:} \quad \alpha = 7.6 \times 10^{-36} E^6 \quad (7)$$

where E is the electric field. It is worth pointing out that the above equations are not a fit to the  $\alpha_p$  versus E data, but are derived to allow analytical calculations of the breakdown voltage for 4H and 6H-SiC devices with the same values as those obtained by simulations performed using Chynoweth's equation with  $a_p$  and  $b_p$  values from Table I. Using the equations for the electric field distribution in a depletion region [3] and using the breakdown condition (i.e.  $\int \alpha dx = 1$ ) we obtain the following relationship for 6H and 4H-SiC:

$$\text{6H-SiC:} \quad W_{c,pp} = 8.2 \times 10^{10} N_D^{-6/7} \quad (8)$$

$$\text{4H-SiC:} \quad W_{c,pp} = 9.0 \times 10^{10} N_D^{-6/7} \quad (9)$$

where,  $W_{c,pp}$  is the parallel plane depletion layer width at breakdown. Using the depletion layer width at breakdown from Eqn. (8) and Eqn. (9), the critical electric field at breakdown for 6H and 4H-SiC was derived to be:

$$\text{6H-SiC:} \quad \epsilon_{c,pp} = 1.52 \times 10^4 N_D^{1/7} \quad (10)$$

$$\text{4H-SiC:} \quad \epsilon_{c,pp} = 1.64 \times 10^4 N_D^{1/7} \quad (11)$$

Also, using the depletion widths from Eqn. (8) and Eqn. (9), the avalanche breakdown voltage ( $BV_{pp}$ ) in an abrupt 6H and 4H-SiC junction diode was derived to be:

$$\text{6H-SiC:} \quad BV_{pp} = 6.3 \times 10^{14} N_D^{-5/7} \quad (12)$$

$$\text{4H-SiC:} \quad BV_{pp} = 7.5 \times 10^{14} N_D^{-5/7} \quad (13)$$

Simulations were performed using MEDICI to obtain the breakdown voltages for a parallel plane 6H and 4H-SiC Schottky structures for various doping concentrations using the ionization coefficients obtained from the P-EBIC technique. We can see from Fig. 9, which

compares the breakdown voltages for various doping concentrations obtained from the simulations to that obtained from Eqn. (12) and Eqn. (13), that the analytical equations work well in the doping ranges  $1 \times 10^{15} / \text{cm}^3$  to  $1 \times 10^{17} / \text{cm}^3$  for both 4H and 6H-SiC, with less than 5% difference in the breakdown voltage calculated from Eqn. (9) to that calculated from simulation. A comparison of the electric field values and depletion widths obtained from simulation for 6H and 4H-SiC to the values obtained from the above equations is provided in Fig. (10) and Fig. (11). The analytical equations fit the simulated values very well for all the junction parameters. It is important to note that these analytical solutions were derived from measurements made on defect free structures. The breakdown voltage and critical electric field strength values reported in literature on fabricated 6H and 4H-SiC diodes are also shown in Fig. 9 and Fig. 10 [4,8], respectively. The scatter in the experimental data is an indication of variable material quality due to the presence of defects. We believe that, in comparison with our analytical solutions, the experimentally measured values are lower because of the presence of defects and enhanced electric field at the edges. Our equations and plots are useful for obtaining the background doping level and minimum drift region width required to achieve the breakdown voltage being designed for any silicon carbide power device. The expressions given above also provide useful normalization parameters for analysis of various junction terminations.

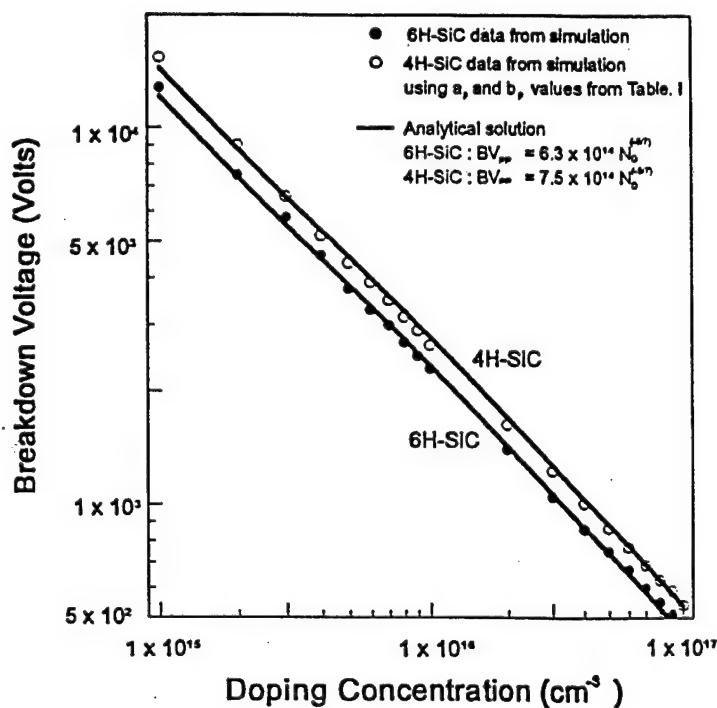


Figure 9. Comparison of the breakdown voltages obtained from the analytical equations to the values obtained from simulations for a parallel plane 6H and 4H-SiC Schottky diode.

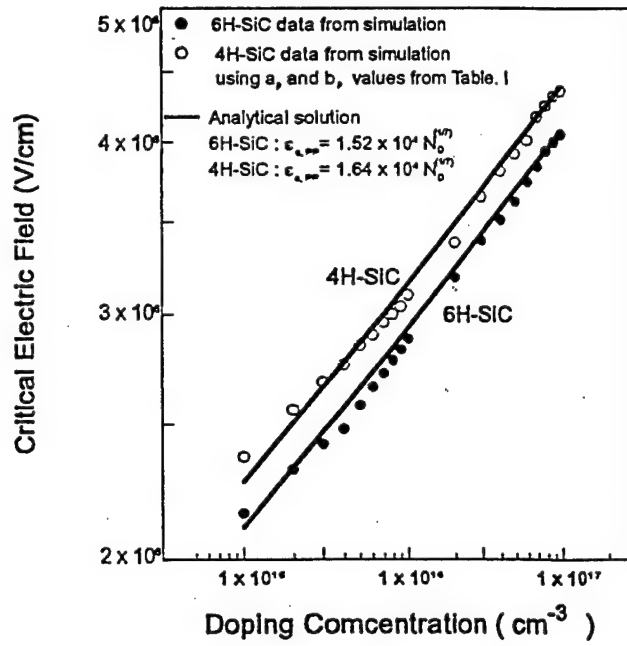


Figure 10. Comparison of the critical electric field values obtained from the analytical equations to the values obtained from simulations for a parallel plane 6H and 4H-SiC Schottky diode.

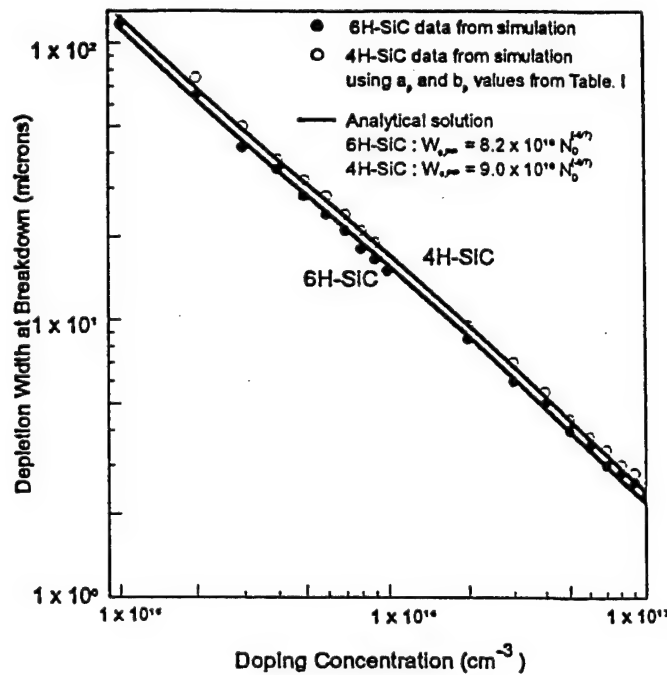


Figure 11. Comparison of the depletion width at breakdown obtained from the analytical equations to the values obtained from simulations for a parallel plane 6H and 4H-SiC Schottky diode.

## G. Conclusions

The impact ionization coefficient  $\alpha_p$  has been accurately measured as a function of temperature in both 4H and 6H-SiC using the P-EBIC technique. The  $\alpha_p$  values obtained for 6H-SiC are lower than the previously reported data. This implies a 15% increase in the breakdown field strength ( $E_c$ ) for 6H-SiC and a 20% increase in  $E_c$  for 4H-SiC. Using this data, it is found that Baliga's Figure of Merit (BFOM) increases by about 1.5 x in 6H-SiC and by about 1.8 x in 4H-SiC indicating even superior specific on resistance for SiC FETs than projected earlier [19]. The impact ionization coefficient  $\alpha_p$  was found to follow the Chynoweth's law over a broad range of the electric field. An analytical equation was derived for the variation of  $\alpha$  with  $E$ , which allowed us to obtain close-formed solutions for breakdown voltage in 6H and 4H-SiC with the same values as that obtained using the Chynoweth's equation.  $\alpha_p$  was found to decrease with increasing temperature indicating a positive temperature coefficient for breakdown for 4H and 6H-SiC. This is a very desirable property for power devices as it ensures safe reliable operation of the device. The negative temperature coefficients for breakdown voltage reported in the literature are probably due to the presence of defects in the SiC material.

## H. Acknowledgments

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## V. Lateral N-channel Inversion Mode 4H-SiC MOSFETs

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Advances in MOS devices on SiC have been greatly hampered by the low inversion layer mobilities. In this paper, the electrical characteristics of lateral n-channel MOSFETs fabricated on 4H-SiC are reported for the first time. Inversion layer electron mobilities of  $165 \text{ cm}^2/\text{V}\cdot\text{s}$  in 4H-SiC MOSFETs were measured at room temperature. These MOSFETs were fabricated using a low temperature deposited oxide, with subsequent oxidation anneal, as the gate dielectric.

### A. Introduction

Silicon carbide (SiC) has been projected to be an excellent semiconductor for the fabrication of devices for high frequency and high temperature applications [1]. The advantages of silicon carbide MOSFETs over their silicon counterparts for high power applications has also been projected [2]. However, the low inversion layer mobilities measured in 6H-SiC (the highest value reported is  $72 \text{ cm}^2/\text{V}\cdot\text{s}$  [3]) have resulted in high channel contributions to the on-resistance leading to higher than expected on-state drops for power MOSFETs. Further, to our knowledge lateral MOSFETs on 4H-SiC have not been reported in the literature. In this paper, we wish to report the successful fabrication of lateral MOSFETs in 4H-SiC with high inversion layer mobilities.

### B. Fabrication

The MOSFETs were fabricated using a non-selfaligned process. The SiC wafers used in this work was aluminum doped P<sup>-</sup> epitaxial layer with a nominal doping of  $2.5 \times 10^{15} \text{ cm}^{-3}$  grown on P<sup>+</sup> 4H-SiC substrates [4]. The wafers were initially given a standard RCA clean without a subsequent HF dip. The wafers were then subjected to the following oxidation cycle: dry oxygen at  $1050^\circ\text{C}$  for 5 minutes, steam at  $1050^\circ\text{C}$  for 265 minutes and again in dry oxygen at  $1050^\circ\text{C}$  for 5 minutes. The 220Å thick thermal oxide was removed by etching in dilute HF and the wafers were then cleaned using an RCA clean without a final HF dip. A low temperature oxide (LTO) of thickness about 8000Å was deposited on the wafers and patterned to define the drain and source regions. The LTO deposition temperature was  $410^\circ\text{C}$  and the chamber pressure was 750 milliTorr during the deposition. The flowrates were 150sccm of  $\text{O}_2$  and 75sccm of LTO-410 (disilane). After etching the source-drain windows, a second LTO of thickness 1000Å was deposited under identical conditions to act as the pad oxide during the

subsequent high dose, high temperature, nitrogen implants ( $80\text{keV}:2\times 10^{15}\text{cm}^{-2}$ ,  $40\text{keV}:1\times 10^{15}\text{cm}^{-2}$  at  $1000^\circ\text{C}$ ) performed to create these drain-source regions. The wafers were annealed in Ar at  $1250^\circ\text{C}$  for 60 minutes to activate the implants. The LTO was then subjected to an oxidation anneal in  $\text{N}_2$  bubbled through DI water at  $98^\circ\text{C}$  at  $1100^\circ\text{C}$  for 400 minutes, an in situ Ar anneal at  $1100^\circ\text{C}$  for 60 minutes, followed by a  $950^\circ\text{C}$  wet  $\text{N}_2$  anneal for 60 minutes. The anneal was performed to densify this oxide and reduce the interface state density [3]. Subsequent to this oxidation anneal, 4000Å of polysilicon was deposited on the wafers and degenerately doped with phosphorus using phosphorus disks in nitrogen at  $875^\circ\text{C}$  for 60 minutes. The polysilicon was patterned into the gates and Al metal contacts to the drain, gate and source were achieved using lift-off. An oxide etch in buffered HF was performed after the lithography and immediately prior to metallization to remove any pad oxide on the polysilicon or SiC. MOSFETs were fabricated with nominal gate widths of  $170\text{ }\mu\text{m}$  and nominal gate lengths of 5, 20, 40, and  $80\text{ }\mu\text{m}$ . The structural cross-section of the MOSFET is shown in the inset of Fig. 3. Quasistatic and 100kHz capacitance-voltage (C-V) measurements were performed on MOS capacitors on the wafer using a Keithley Model 82 simultaneous system. Current-voltage (I-V) measurements were made on the FETs using a Keithley Model 251 test system.

### C. Results and Discussion

C-V measurements on MOS capacitors showed an average  $N_{\text{eff}}$  of  $5\times 10^{11}\text{ cm}^{-2}$  and confirmed the LTO thickness at about 9000Å. The I-V output characteristics of a typical 4H-SiC MOSFET ( $W/L=170\mu\text{m}/82.5\mu\text{m}$ ) at 300K upto a gate bias of 10V are shown in Fig. 1. The device exhibits excellent gate controlled linear and saturation regimes of operation. To discount the possibility of conduction in a buried channel in the FETs, the output characteristics upto a gate voltage of 70V for a MOSFET ( $W/L=170\mu\text{m}/40.5\mu\text{m}$ ) were measured at 300K and are shown in Fig. 2. We believe that the continued reduction in resistance at higher gate bias provides evidence that a bulk conduction path does not exist in these devices. Gate leakage was substantial at gate biases higher than 70V because, while the gate oxide above the substrate is about 9000Å thick, the gate oxide above the highly doped drain source overlap region is much thinner (1000Å) [5]. This limited the maximum gate bias to 70V. The threshold voltage for all MOSFETs was determined from the intercept on the  $V_G$  axis made by the tangent to the transfer characteristics of the MOSFET at the point of inflection as shown in Fig. 3 for the same FET as in Fig. 1. The threshold voltage was measured to be between 0-0.5V for all measured FETs which was corroborated by the measured  $N_{\text{eff}}$  and LTO thickness on the capacitors. These FETs had an unusually large gate oxide thickness of 9000Å because they were laid out to measure the threshold voltage of FETs fabricated on field oxide.

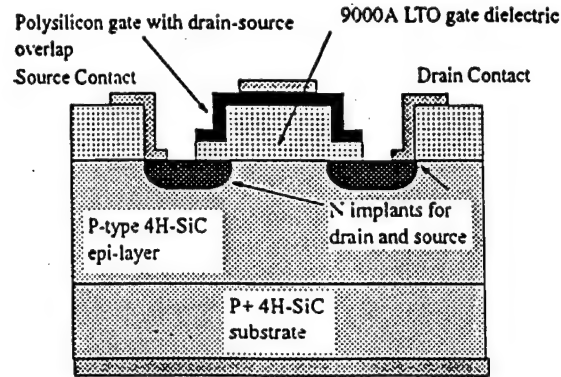


Figure 1. Measured output characteristics at 300K of a 4H-SiC n-channel inversion mode lateral MOSFET with W/L ( $170\ \mu\text{m}/82.5\ \mu\text{m}$ ) at gate bias upto 10V. Threshold voltage is 0V.

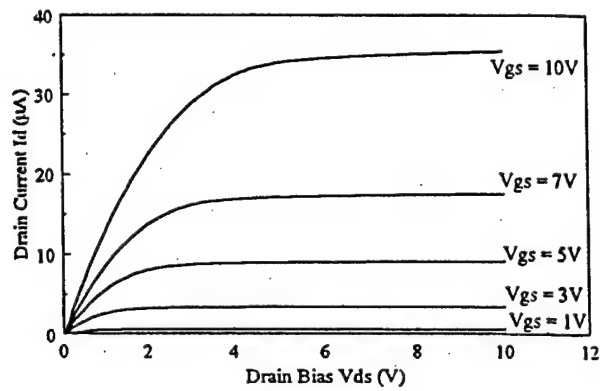


Figure 2. Measured output characteristics at 300K of a 4H-SiC n-channel inversion mode lateral MOSFET with W/L ( $170\ \mu\text{m}/40.5\ \mu\text{m}$ ) at different gate biases up to 70V.

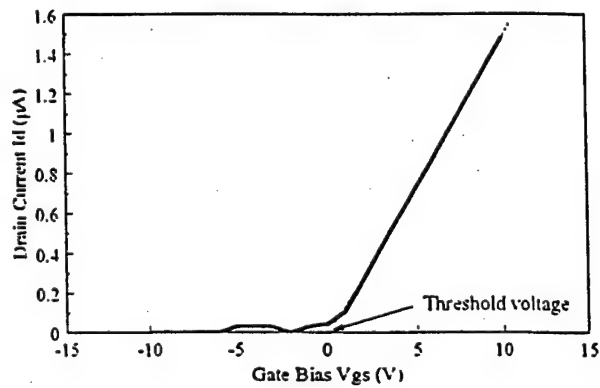


Figure 3. Measured transfer characteristics at 300K of a 4H-SiC n-channel inversion mode lateral MOSFET with W/L ( $170\ \mu\text{m}/82.5\ \mu\text{m}$ ) at a drain bias of 100mV. The inset shows the structure of the fabricated non self-aligned FET.

The maximum inversion layer mobility of  $165 \text{ cm}^2/\text{V}\cdot\text{s}$  was extracted from the linear region of the output characteristics ( $V_{DS} = 100\text{mV}$ ) based on the Equation:

$$\mu_n = \frac{\frac{\partial I_D}{\partial V_{DS}}}{C_{ox} \frac{W}{L} (V_{gs} - V_{th})}$$

The plot of inversion layer mobilities at low gate biases for 4H-SiC MOSFETs using the MOSFETs of different channel lengths is shown in Figure 4. It can be seen that an electron inversion layer mobility of  $165 \text{ cm}^2/\text{V}\cdot\text{s}$  at a gate bias of  $8\text{V}$  is consistently measured on these MOSFETs. The measured higher inversion layer mobility in 4H-SiC compared to the reported values in 6H-SiC is consistent with the higher bulk mobility for 4H-SiC in the (0001) plane [6]. We speculate that the use of a deposited oxide as the gate dielectric, in conjunction with appropriate densification anneals in both oxidizing and inert ambients, resulted in reduced surface effective charge densities and interfacial nonuniformities. The accumulation of aluminum in thermally grown oxide on aluminum doped P-type SiC has been studied previously [7] and some authors have opined that this incorporation of Al adversely affects the interface disorder and oxide charge density [8]. Therefore the use of deposited oxides would allow the reduction of the above and the consequent increase in inversion layer mobility. The extracted inversion layer mobility was found to decrease to  $115 \text{ cm}^2/\text{V}\cdot\text{s}$  at a gate bias of  $70\text{V}$ . This 30% reduction with increase in the normal field in the gate oxide by a factor of 10x (from  $0.8$  to  $8 \times 10^5 \text{ V/cm}$ ) is not as severe as the 30% reduction reported previously for 6H-SiC for an increase in normal field in the gate oxide by a factor of 2x (from  $1.7$  to  $3.4 \times 10^5 \text{ V/cm}$ ) [3]. We believe that the results of our work can be utilized for fabrication of lateral MOSFETs in 4H-SiC for CMOS ICs as well as for planar power MOSFETs.

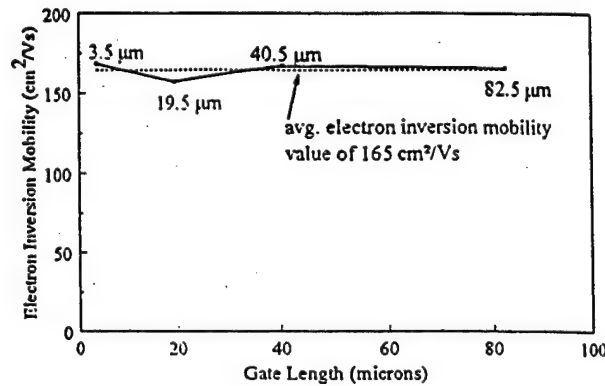


Figure 4. Measured inversion layer mobility of electrons at 300K of 4H-SiC n-channel inversion mode lateral MOSFETs at a gate bias of  $8\text{V}$ .

#### D. Acknowledgements

This work was supported by ARPA under Contract # N00014-95-1-1080 and by the industrial sponsors of the Power Semiconductor Research Center.

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## VI. Electrical Characteristics of Tantalum and Tantalum Carbide Schottky Diodes on n- and p-type Silicon Carbide as a Function of Temperature

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This study reports on the electrical stability of Ta/SiC and TaC/SiC interfaces at potential device operating temperatures (25 to 400°C). In contrast to previous reports on thermal stability of contacts, which report the electrical properties after high temperature annealing, this study reports the electrical properties of contacts measured both at room temperature (prior to and subsequent to annealing) and at elevated temperatures in air.

Tantalum on p-type 6H-SiC (0001) showed good diode characteristics with low reverse leakage currents to 350°C ( $\leq 5 \times 10^{-7}$  A/cm<sup>2</sup> at 5 V). The results indicate that current transport across the interface is dominated by thermionic emission only at temperatures above 300°C. The ideality factors decreased from 2.24 at R.T. to 1.07 at 400°C. Thus, Schottky barrier heights (SBH's) calculated from these measurements are believed to be underestimated for the lower temperatures, where current transport is believed to be dominated by recombination. On n-type 4H-SiC, Ta contacts also displayed good diode behavior at 25°C with significant increases in reverse leakage at temperatures as low as 100°C.

As expected from its low work function (Fomenko, 1966; Kosolapova, 1971), TaC on lightly doped ( $4.1 \times 10^{16}$  cm<sup>-3</sup>) n-type SiC resulted in leaky diodes at R.T. These contacts showed ohmic behavior at temperatures above 200°C. Tantalum carbide contacts on p-type ( $2 \times 10^{15}$  cm<sup>-3</sup>) material displayed diode behavior with low reverse leakage currents to 250°C.

Good reversibility of the current-voltage characteristics of all of these contacts after cycling between R.T. and 400°C was observed. These results indicate the absence of interfacial reactions and, hence, the potential for thermally stable contacts to 400°C.

### A. Introduction

Silicon carbide has substantial advantages over Si for use in high temperature electronics (Davis, 1993; Morkoç, 1994). However, while its intrinsic, bulk properties allow for the expansion of the current limits on operating conditions in terms of temperature, power, and frequency, interfaces between dissimilar materials at the discrete device level as well as the packaging and interconnection levels often interact at relatively low temperatures.

In selecting contact materials for this study, several physical properties of materials such as work function, melting point, thermodynamic driving force for oxidation, and thermodynamic



stability with SiC were considered. Of these, the thermodynamic stability was the first criterion considered, because contact materials that will be used in continuous operation at high temperatures must not change with time. Contact materials that have tie lines with SiC in the M-Si-C (M=metal) ternary phase diagram do not react at the temperature specified.

This study reports on the electrical properties and stability of Ta/SiC and TaC/SiC interfaces at temperatures between room temperature (R.T.) and 400°C. Tantalum carbide was investigated because of its thermodynamic stability with SiC (Schuster, 1993) and its physical properties (e.g., oxidation properties, melting point and work function). The electrical properties of pure Ta contacts, which has reportedly high reaction temperatures with SiC (Geib *et al.*, 1990; Schuster, 1993; Chen *et al.*, 1994), were compared to those of TaC.

The reversibility of the electrical properties of the contacts after cycling between R.T. and 400°C was investigated to determine their chemical stability. These results are discussed along with the potential application of these contacts for high temperature devices.

## B. Experimental Procedure

Aluminum-doped p-type ( $2 \times 10^{15} \text{ cm}^{-3}$ ) 6H-SiC and nitrogen-doped n-type ( $1.5 \times 10^{16} \text{ cm}^{-3}$ ) 4H- and ( $4.1 \times 10^{16} \text{ cm}^{-3}$ ) 6H-SiC wafers were grown by Cree Research, Inc. The Si-terminated (0001) vicinal ( $3.5^\circ$  off axis for 6H,  $8^\circ$  for 4H) surfaces were used as the substrate for all metal depositions. The substrates were cleaned using acetone (5min) and methanol (5min). The thermally grown oxide layers were etched from the surface using a 10 min. dip in a 10% hydrofluoric acid solution. This step was followed by a quick rinse in de-ionized water and drying with  $\text{N}_2$ . The substrates were loaded into a d.c. sputtering system and thermally desorbed at 550°C for 10 min. at base pressure of  $<3.0 \times 10^{-7}$  Torr to remove hydrocarbon contamination from the substrate surfaces.

A d.c. sputtering system with a base pressure of  $<3.0 \times 10^{-7}$  Torr was used to deposit Ta and TaC films (thickness of 2000 Å). Prior to each deposition a 2 min. pre-sputter was performed to remove foreign material from sputtering target surface. Each substrate was shuttered during this pre-sputtering. For ohmic contacts, 3000 Å of Ti-Al (10-90 wt. %) or Ni was deposited on the backside of the p- and n-type substrates, respectively, and annealed at 900°C for 5 min. in a rapid thermal annealing furnace.

Contact structures consisting of 0.02" and 0.03" diameter circular contacts were created for electrical characterization by depositing the metal through a Mo mask in contact with the substrate. Current-voltage (I-V) measurements were taken with an HP 4155A semiconductor parameter analyzer. The I-V characteristics of the samples were measured in air at temperatures between 25 and 400°C in 50°C increments with the use of a Signatone S-1160 high temperature prober. The samples were held at each temperature for an average time of 10 min.

### C. Results

*Ta on p-type 6H-SiC.* Tantalum contacts on lightly doped p-type SiC displayed very low reverse leakage currents at temperatures to 350°C (Fig. 1). The forward resistance decreased with temperature. As shown in Fig. 2, the reverse leakage increased with temperature. The reverse I-V traces at 25, 100, and 150°C were similar to the results shown for 200°C and were excluded from the Figure for clarity. At a reverse bias of 10 V, the current densities through the contact were  $2.4 \times 10^{-9}$  and  $1.2 \times 10^{-4}$  A/cm<sup>2</sup> at R.T. and 400°C, respectively.

Some indication of the dominant current transport mechanisms can be obtained by plotting the forward current on a logarithmic scale. For thermionic emission of carriers over the Schottky barrier, the current has an exponential dependence on voltage for  $V > 3kT/q$  (and to the point where the current is limited by the resistance of the device). Thus, by plotting  $\log I$  vs.  $V$ , a linear relationship is obtained. The closeness of the diode behavior to the thermionic emission model is quantified by an ideality factor ( $n$ ), which can be calculated from the slope of the  $\log I$  vs.  $V$  plot. When thermionic emission is the dominant current transport mechanism,  $n$  is close to 1.0. Figure 3 shows the  $\log I$ - $V$  curves for these Ta contacts as a function of temperature. As expected, the current at a fixed voltage increases with temperature. The ideality factors calculated from these curves decreased from 2.24 at R.T. to 1.07 at 400°C (Table 1). The calculations indicate that thermionic emission is not the dominant current transport mechanism for these contacts at temperatures below ~300°C. This result is likely due to a large

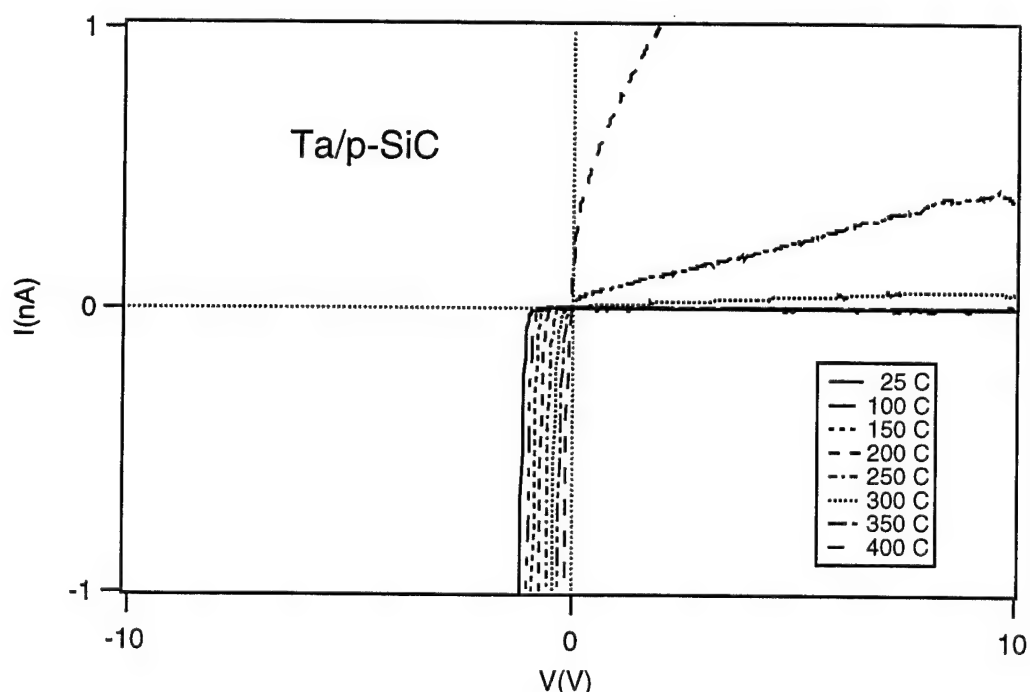


Figure 1. Current-voltage measurements of Ta / p-type 6H-SiC Schottky diodes as a function of measurement temperature.

Table I. Ideality Factors ( $n$ ) and Schottky Barrier Heights ( $\Phi_B$ ) Calculated from I-V Measurements of Ta on p-type ( $2 \times 10^{15} \text{ cm}^{-3}$ ) 6H-SiC (0001) as a Function of Temperature

T (°C)	$n$	$\Phi_B$ (eV)
25	~2.2	—
100	1.86	—
150	1.70	—
200	1.51	—
250	1.32	—
300	1.18	~1.95
350	1.09	1.96
400	1.07	2.04

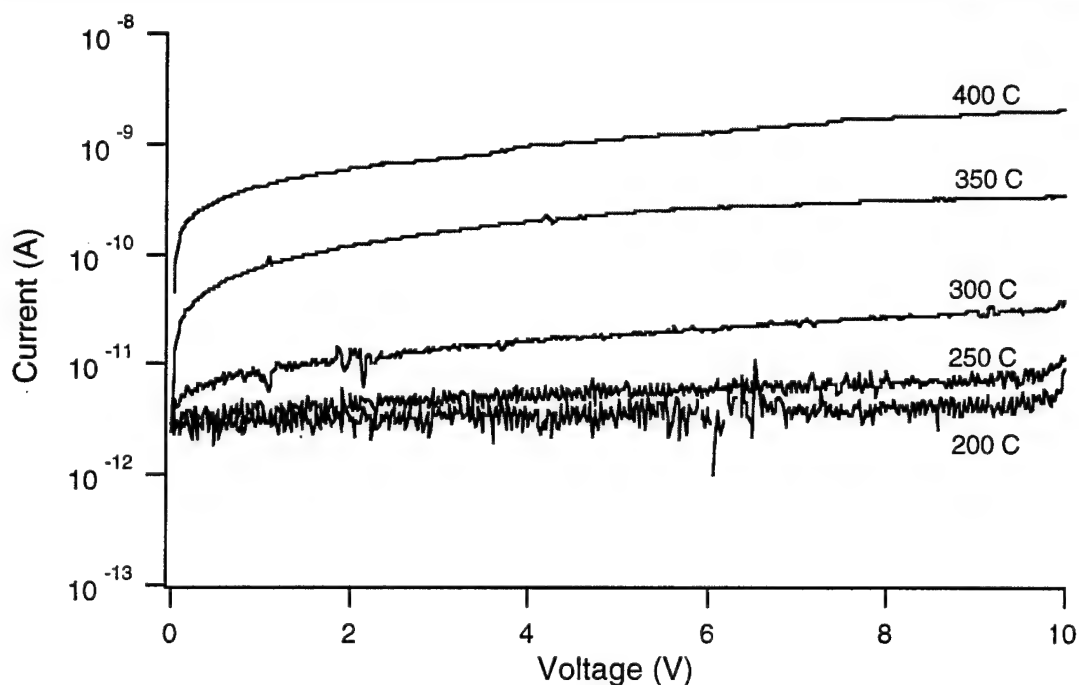


Figure 2. Current at reverse bias of Ta / p-type 6H-SiC diode as a function of temperature.

Schottky barrier height, as calculated at the higher temperatures, and/or defects in the p-type material, which could result in recombination in the depletion region. It is expected that recombination becomes less significant with increasing temperature (Rhoderick and Williams, 1988). Thermionic field emission is probably not significant because of the low tunneling coefficient for SiC at this doping level. Further analysis of the data will be performed to quantitatively determine the current transport mechanisms as a function of temperature.

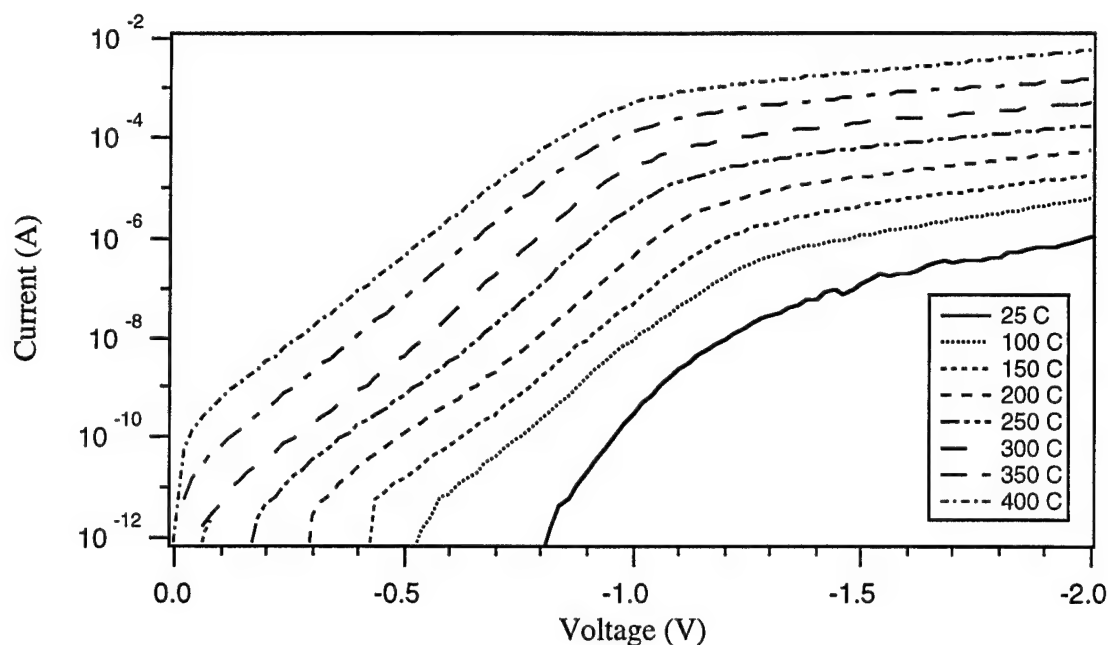


Figure 3. Log I – V curves of Ta / p-type 6H-SiC Schottky diodes as a function of measurement temperature. The curves shift to lower voltages with increasing temperature.

The calculated Schottky barrier heights (SBH's) increased with temperature, which is in qualitative agreement with the results obtained by Smith *et al.*, 1996, from capacitance-voltage measurements; however, the SBH's are believed to be underestimated for the lower temperature measurements, where current transport is more likely dominated by recombination. Thus, an actual increase in SBH with temperature cannot be deduced from the I-V measurements.

The reversibility of the Ta / p-SiC diodes were investigated by comparing the I-V characteristics at R.T. before and after cycling from R.T. to 400 °C. Representative curves displayed in Fig. 4 show that the characteristics were reversible after ten cycles. These results indicate an absence of chemical reactions for these annealing conditions.

*Ta on n-type 4H-SiC.* At room temperature some of these contacts displayed very good diode characteristics with reverse leakage of  $7.45 \times 10^{-9}$  A/cm<sup>2</sup> at -10 V and an ideality factor of 1.03. The average SBH of these contacts was calculated to be 1.03 eV. Ohmic or ohmic-like behavior observed for the other contacts is attributed to micropipes in the substrate, which were observed with the use of an optical microscope.

Measurement of the diodes from 25 to 400 °C showed reversible changes in the electrical characteristics with temperature. The behavior was qualitatively similar to that observed for Ta on p-type 6H-SiC (Fig. 1) with higher currents for the n-type samples at elevated temperatures than observed for p-type samples. This result is attributed to smaller SBH's for Ta on n-type substrates than on p-type substrates.

*TaC on n-type 6H-SiC.* Because of its low (3.9 eV) work function (Fomenko, 1966; Kosolapova, 1971), TaC was investigated as a potential ohmic contact for n-type SiC. On lightly doped ( $4.1 \times 10^{16} \text{ cm}^{-3}$ ) n-type 6H-SiC, the TaC contacts resulted in leaky diodes at R.T. These contacts showed ohmic behavior at temperatures above 200°C (Fig. 5). In further investigations, TaC will be deposited on more highly doped substrates, for which ohmic behavior is expected. Specific contact resistivities of the ohmic contacts will be calculated as a function of temperature. These contacts also displayed reversible characteristics after several heating cycles between R.T. and 400°C, a result which is attributed to the thermodynamic stability of TaC with SiC (Schuster, 1993).

*TaC on p-type 6H-SiC.* Tantalum carbide contacts on p-type ( $2 \times 10^{15} \text{ cm}^{-3}$ ) material displayed diode properties with low reverse bias currents to 250°C, as shown in Fig. 6. The I-V characteristics for these diodes were qualitatively similar to the results shown in Figures 2–4 for Ta contacts on p-SiC. An ideality factor of 1.49 was calculated for contacts measured at R.T., again indicating that thermionic emission is not the dominant current transport mechanism. Thus, the 2.1 eV value calculated from these measurements may be an underestimate of the SBH.

The TaC contacts also showed reversibility after ten heating cycles from R.T. to 400°C, indicating the absence of chemical reactions and, hence, the potential as a thermally stable contact material for temperatures to 400 °C. Long-term annealing of these contacts at higher temperatures in an inert ambient will be performed in the future to further test their stability.

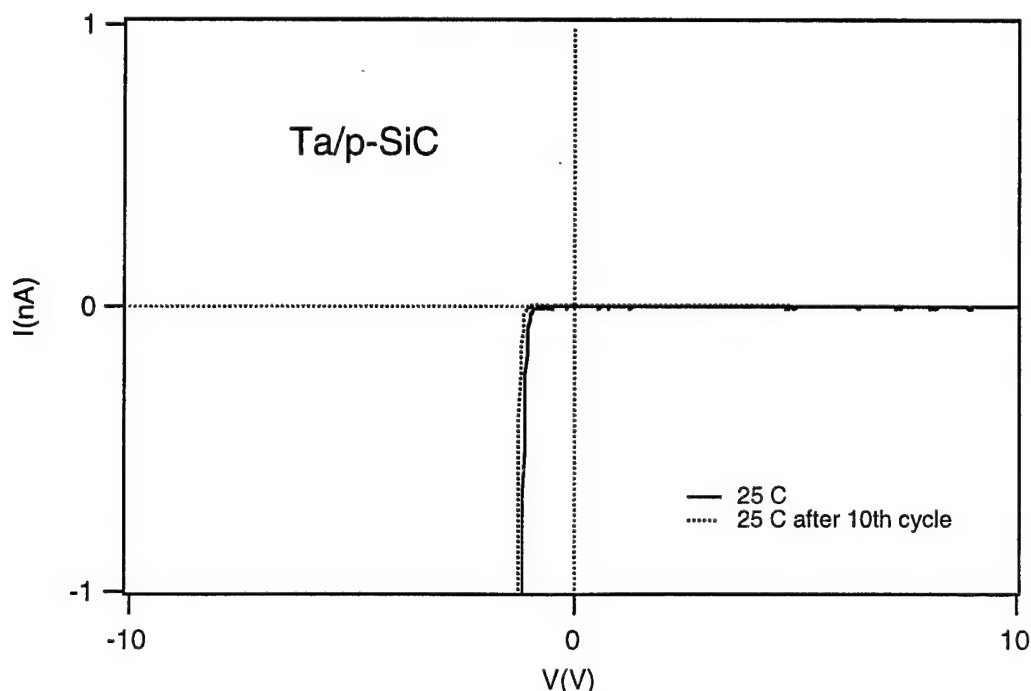


Figure 4. Current-voltage measurements of Ta on p-type 6H-SiC in the as-deposited condition and after ten heating cycles from R.T. to 400°C.

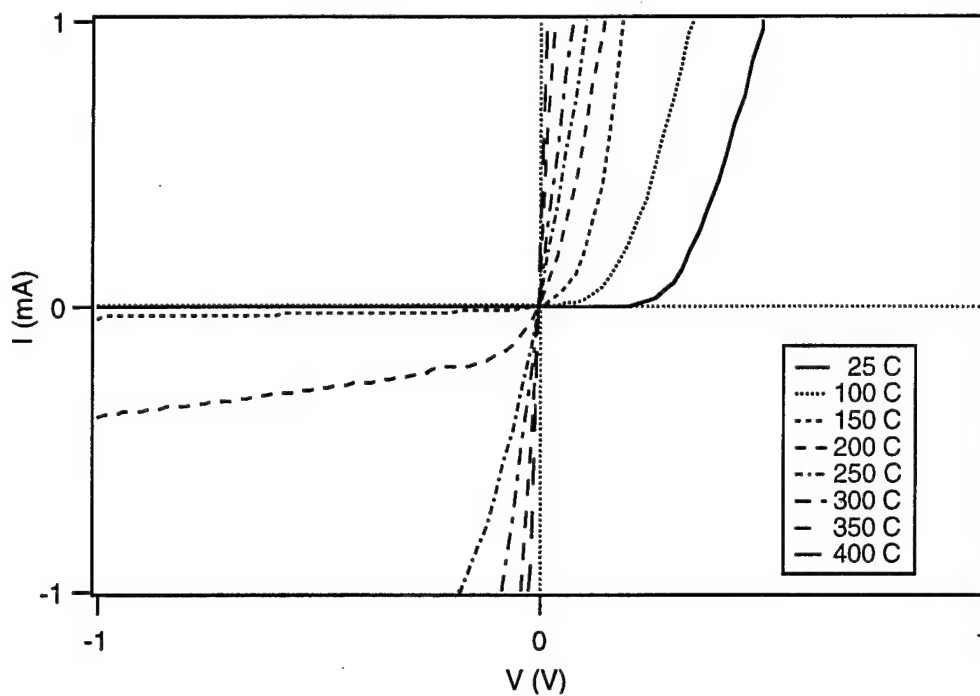


Figure 5. Current-voltage measurements of TaC / n-type 6H-SiC as a function of measurement temperature.

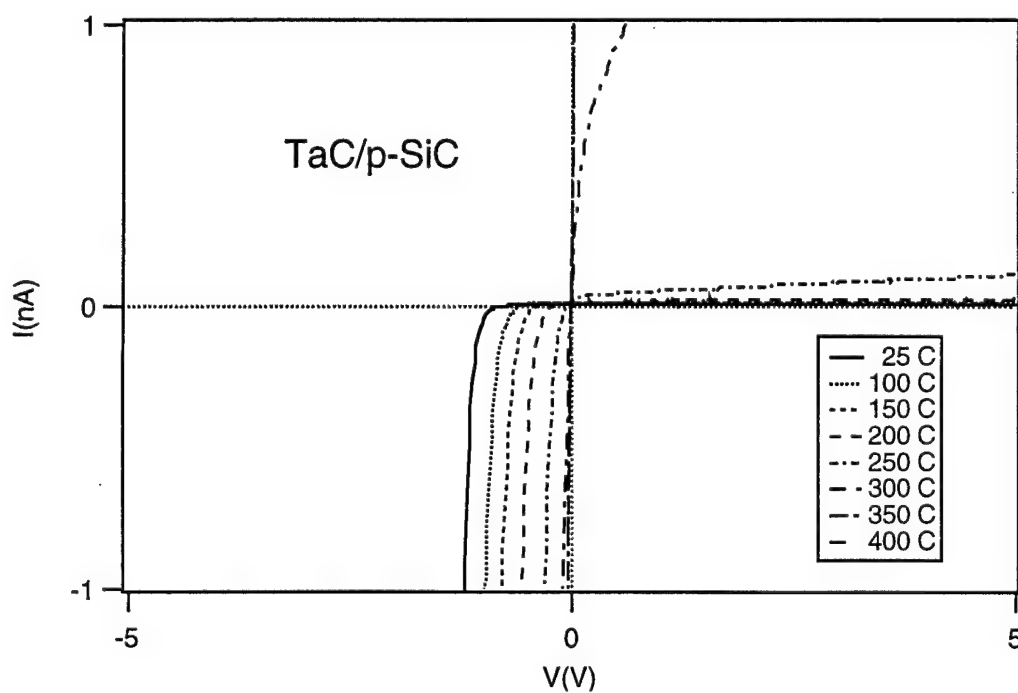


Figure 6. Current-voltage characteristics of TaC on p-type 6H-SiC as a function of measurement temperature.

#### D. Summary

The thermal stability of TaC and Ta contacts on n- and p-type SiC was investigated by measuring the I-V characteristics in air at temperatures between 25 and 400 °C. Changes in the electrical characteristics with measurement temperature were investigated. All of the contacts showed reversibility after up to the maximum number (ten) of heating cycles performed, indicating an absence of chemical reactions. Hence, the potential exists for the use of these materials as thermally stable contacts to SiC at temperatures to 400°C. While TaC is reported to be thermo-dynamically stable with SiC, Ta is not. Thus, longer-term annealing of these contacts should be performed to determine whether the kinetics of the interfacial reactions are slow enough for their practical application at these temperatures or whether other effects may degrade the electrical properties over time.

#### E. Acknowledgement

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## VII. Examination of the Silicon – Silicon Carbide Interface by Ultraviolet Photoemission Spectroscopy

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Ultraviolet photoemission spectroscopy (UPS) was used to investigate the interface properties of 6H-SiC. Both deposited silicon and silicon dioxide were investigated. Silicon carbide cleaned in  $\text{SiH}_4$  flux from a gas source molecular beam epitaxy (GSMBE) system was used for this study. All processes were accomplished in an ultra high vacuum integrated system that allowed all cleaning, deposition, and analysis to be completed without exposure to ambient atmosphere. Sub- to multiple monolayers of silicon were deposited on SiC and approximately  $10\text{\AA}$  of oxide was formed on SiC via O-plasma and the valence band structure was investigated. The valence band maximum (VBM) was observed to shift for Si depositions greater than 1 monolayer. The VBM offset was determined to be  $+2.4\text{eV}$  for a layer of  $60\text{\AA}$  Si on SiC. Furthermore, the VBM was observed to shift for O-plasma treatment. The VBM offset was determined to be  $-1.9\text{eV}$  for approximately  $10\text{\AA}$  layer of  $\text{SiO}_2$ . The results are discussed in terms of the two interfaces.

### A. Introduction

Silicon carbide is a wide band gap semiconductor, which is often considered the material of choice for high-power, high-temperature device applications. Among the different polytypes, the hexagonal structure (6H or 4H) is of main interest due to physical properties such as large band gap, high thermal conductivity and electron mobility, and superior growth quality. The electronic properties of the Si-SiC interface are of interest for MESFET applications with a heterojunction gate. Band bending behavior, band discontinuities and surface state distribution are key considerations for a device-sufficient interface design. Poly Si gated SiC high power devices show nonideal blocking performance [1], which may be due to the electronic structure of the interface. The properties of the  $\text{SiO}_2$ -SiC interface are of interest for MOS applications with a  $\text{SiO}_2$  gate. Interface state, fixed oxide charge, and blocking performance are an integral part of incorporating SiC as a viable material for power devices.

### B. Experimental Procedure

The substrate used was a quarter wafer of on axis, n-type 6H SiC ( $N_D - N_A = 2 \times 10^{18} \text{ cm}^{-3}$ ) supplied by Cree Research, Inc. The wafer was wet chemically cleaned with a SC1 etch ( $5:1:1 \text{ H}_2\text{O}:\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$ ) at room temperature for 10 min. to remove polishing residues. A UV/ $\text{O}_3$  treatment followed by a  $10:1$  HF-dip and DI-rinse removed surface organics from the SiC.

To obtain a sufficient thermal contact for successive heating steps in UHV, tungsten was sputtered on the backside. The final wet chemical processing consisted of two UV/O<sub>3</sub>-HF dip-DI rinse processes. Finally, the sample was mounted with tantalum wires on a molybdenum sample holder and loaded into an integrated UHV-system ( $p_{\text{Base}}=1\times 10^{-9}$  Torr) which has a series of cleaning, analysis and deposition stations described elsewhere [2]. The efficacy of the wet chemical cleaning was monitored by Auger electron spectroscopy (AES) and low energy electron diffraction (LEED). After the final HF etch, a thin oxide layer is bonded to the surface and a  $1\times 1$  LEED pattern was observed. The electronic structure of the as-loaded surface was measured with UPS. For further cleaning purposes, the sample was annealed to  $>900^{\circ}\text{C}$  in a SiH<sub>4</sub>-flux to prevent surface carbonization [3]. The oxygen content on the surface was reduced below the detection limit of AES, and the silicon-rich surface exhibited a sharp, well-defined  $1\times 1$  LEED pattern at  $E_{\text{B}}=50\text{eV}$ .

After this initial surface preparation the sample was examined by ultraviolet photoemission spectroscopy (UPS) measurements. A differentially pumped noble gas resonance lamp was used. The lamp was operated with helium and is optimized for the He I alpha regime,  $E_0=21.22\text{ eV}$ . During lamp operation the pressure in the UPS chamber increased to  $8\times 10^{-9}$  Torr, but the increased He partial pressure is not expected to cause sample contamination. The photo emitted electrons are analyzed with a VSW HA50 hemispherical analyzer ( $r_{\text{mean}}=50\text{mm}$ ) which operated at an energy resolution of  $0.15\text{ eV}$ . The spectrometer was mounted on a double angle goniometer to measure the dispersion of photoelectrons with respect to the surface normal. The energy distribution of the emitted photoelectrons was determined over a range from 0 to  $18\text{ eV}$ . UPS allows measurement of the electron affinity,  $\chi$ , for semiconductors with known band gap values. To obtain the spectral width and, therefore, the electron affinity, a  $-2\text{V}$  bias was applied to the sample with respect to ground. The bias was necessary to overcome the work function of the analyzer. All UPS spectra were normalized to the Fermi level of the system. The Fermi level was determined by measuring a clean molybdenum surface in electrical contact with the sample.

Sub monolayer growth of silicon was achieved by employing a molecular beam epitaxy (MBE) system. The growth rate was monitored using oscillating quartz crystals. The silicon was deposited at  $550^{\circ}\text{C}$  with varying thickness from  $0.3\text{\AA}$  to  $60\text{\AA}$ . The processing chamber base pressure was  $\sim 1\times 10^{-10}$  Torr, desorption pressure was at  $<5\times 10^{-10}$  Torr and the deposition pressure was  $<5\times 10^{-8}$  Torr. The increasing coverage of silicon on the SiC was monitored by AES. Ultraviolet photoemission spectroscopy was performed to monitor the valence band transitions with respect to increasing Si thickness.

Oxide growth was performed by exposing the SiC to an oxygen plasma. The growth was done via remote plasma of oxygen at  $250^{\circ}\text{C}$ . AES was performed to determine the composition of the oxide. By performing UPS, the valence band shift was observed.

### C. Results and Discussion

**Si-SiC Interface.** The UPS spectrum of 6H SiC single crystals after a wet chemical is shown in Fig. 1. The VBM of this surface was detected at  $\sim 2.7\text{eV}$  below the Fermi level. This surface was terminated with oxygen. The value of  $2.7\text{eV}$  was consistent with the bulk values of  $E_F - E_V$  for 6H SiC single crystals with the doping level employed in this study. Therefore, after a wet chemical clean, the results indicated an unpinned Fermi level which was likely due to the oxygen termination of the surface.

After high temperature treatment, a prominent feature was observed at  $2.9\text{eV}$  below  $E_F$ . There was no evidence of the in-gap surface state observed by Johansson *et al.*[5] The UPS spectra after several different Si coverages are shown in Fig. 2. To examine the prominent feature more closely, the shape and intensity were analyzed via a peak fitting routine. The feature was extracted from spectra obtained after subsequent silicon depositions up to several monolayers, see Fig. 3.

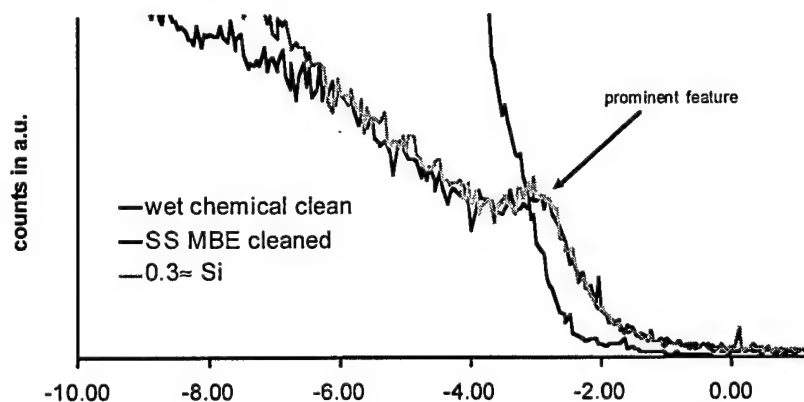


Figure 1. HeI UPS spectrum 6H SiC with different surface modifications.

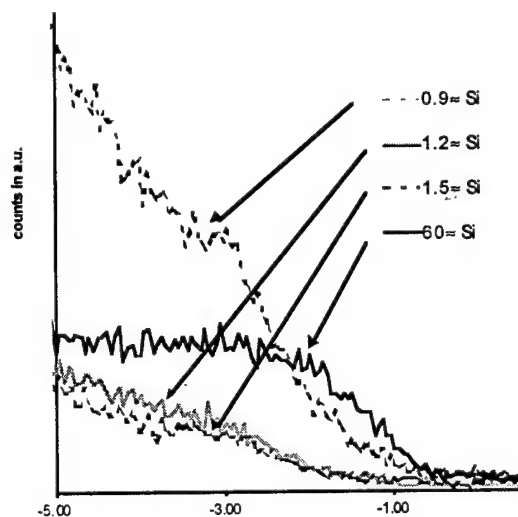


Figure 2. UPS spectrum Si on SiC.

After deposition of  $\sim 1.0\text{\AA}$  Si, the surface state shifted  $\sim 0.4\text{eV}$  towards the valence band edge. The feature was observed to shift back towards  $E_F$  for a Si thickness of  $1.5\text{\AA}$ . Furthermore, peak broadening and a decreasing intensity was observed for increased Si deposition.

It is significant that the prominent feature in the clean SiC UPS spectrum was observed to shift for deposition of Si. Therefore, it is suggested that this feature was actually a surface state or surface resonance because it exhibited a clear dependence from the chemisorbed species (i.e. silicon) [6]. Fulfillment of this non-conclusive criterion [7] seemed to indicate that this feature was probably not caused by direct emission from the VBM as reported by L.I. Johansson *et. al.* [5] for SiC  $\sqrt{3}\times\sqrt{3}$  R30° surfaces. The different peak positions for clean SiC and 1ML Si on SiC surfaces may be explained by a change in the electronic structure of the surface [8].

Determination of the exact position of the VBM of the clean SiC surface was very difficult because emission from the presumed surface state or resonance overwhelmed the actual leading edge of the emission from states at the VBM. The peak fitting and peak removal routines were employed to estimate the actual emission from the valence band maximum. The result of the fitting is shown in Fig. 4. The method yields results in good agreement with expected bulk values [6, 9].

It is suggested that with Si coverage, the system exhibited nearly flat bands in the surface region. It should be pointed out, that the fitting process effectively led to an increase in the margin of error.

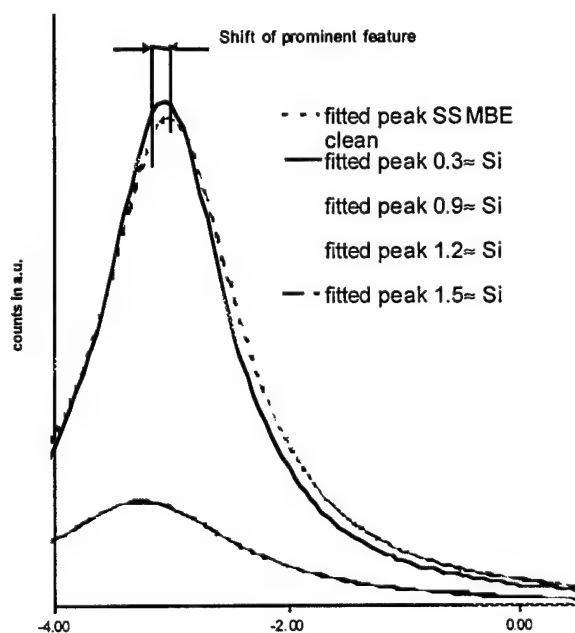


Figure 3. Peak fit of the prominent feature.

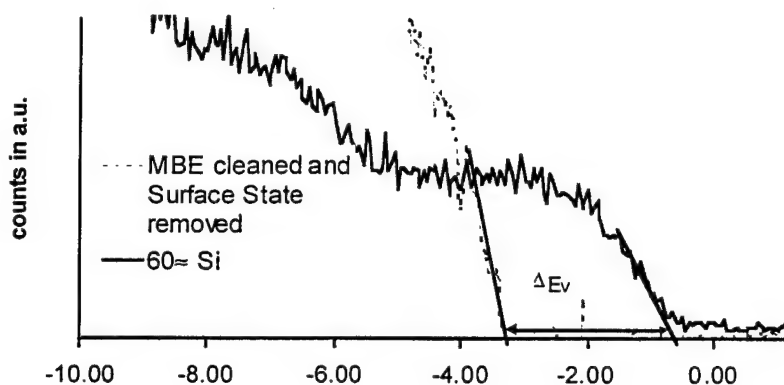


Figure 4. HeI UPS of Si overlayer on SiC compared to the cleaned SiC with the prominent feature removed.

Also shown in Fig. 4, is the UPS spectrum of the Si overlayer. The  $\Delta E_v$  between the valence band max of the SiC and Si overlayer was found to be 2.4 eV. This defined the difference in the valence band but neglected band bending near the interface.

The next aspect to be determined in these measurements was the electron affinity of the SiC and the Si overlayer. The measured spectral width can be related to the electron affinity.

$$\chi = E_{VAC} - CBM = h \cdot f - E_G - W \quad (1)$$

To assure that the width was not limited by the work function of the analyzer, a small bias of 2 V was applied to the sample, and UPS spectra were recorded for the clean SiC surface and the Si overlayer. Affinity values of 4.4 eV and 4.0 eV were obtained for the SiC and silicon overlayer, respectively. These results were in good agreement with previous works [6,9].

A picture could then be constructed of the band alignment as determined by these experiments. The picture that developed is displayed in Fig. 5. Note that the electron affinity measurements determined the conduction band alignment while the valence band UPS determined the valence band alignment. Assuming to first order a transitive relationship for the heterojunction [10] and the electron affinity rule [11] applied, the shift in the conduction band was determined by the electron affinity difference. This would imply for the measured Si-SiC heterojunction a value of 0.4 eV for  $\Delta CBM$ . Note that the results were consistent with the known band gap of Si and SiC. These results were not able to determine the actual band offset at the interface because band bending effects may be significant.

Due to strong emission from surface states, a clear coverage resolved determination of the VBM shift was not feasible. Depletion region width, band offsets and interface state density should also be explored by electrical testing techniques such as current and capacitance versus voltage methods. [12,13].

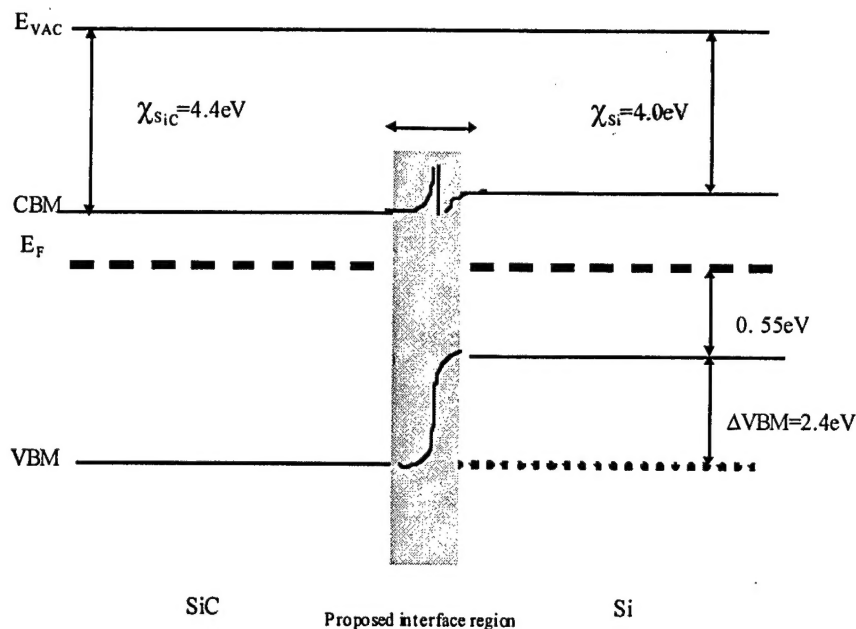


Figure 5. Heterojunction band diagram deduced from measurements presented here.

***SiO<sub>2</sub>-SiC Interface.*** The UPS spectrum after the oxygen plasma, shown in Fig 6, shows a VBM approximately 5.0 eV below the Fermi level. This is in disagreement with previous work by V.V. Afanas'ev, *et al.*[14] They have reported a  $\Delta VBM$  of approximately 3.0 eV. Furthermore, using Eq. 1, it is shown that:

$$\chi + E_g = h\nu - W = 21.2 \text{ eV} - 11.3 \text{ eV} = 9.9 \text{ eV}$$

The generally accepted value for  $\chi + E_g$  for oxide is  $\sim 9.3 \text{ eV}$  ( $\chi = 0.3 \text{ eV}$  and  $E_g = 9.0 \text{ eV}$ ). The difference between the accepted values and the measured values is due to the poor quality of the oxide. The AES spectra showed that the SiC was still detectable through the oxide. Implying that the oxide layer still had considerable carbon within, the AES showed that it was probably a transition stoichiometry between the SiC and the SiO<sub>2</sub>.

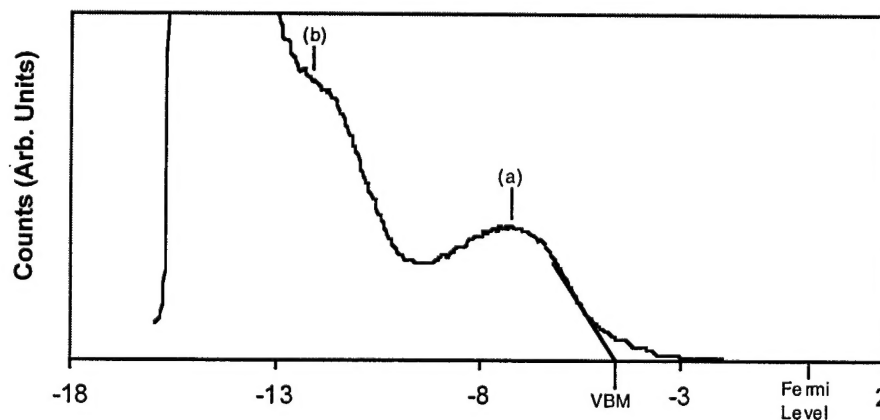


Figure 6. UPS of 6H-SiC after 1min O-Plasma. Note the characteristic oxygen peaks, (a) the O-O bond, and (b) the Si-O bond.

#### D. Conclusions

*Si-SiC Interface.* The electronic structure of 6H SiC after various surface treatments was examined by photoemission studies. The VBM was observed to change with varying Si coverage. The prominent feature at 2.9eV below  $E_F$  was mapped during submonolayer deposition of Si on SiC. The fitted maximum moved towards the expected VBM with successive depositions to 1ML. The VBM approached the expected value of intrinsic Si with 60Å Si overlayer deposition. A value of 2.4eV for  $\Delta VBM$  between 6H SiC and the silicon overlayer was determined, neglecting possible band bending effects. The CBM behavior was determined by measuring the electron affinity for SiC and the Si overlayer. Evaluation of the collected data indicated a CBM offset of 0.4eV.

*Si-SiO<sub>2</sub> Interface.* The electronic structure of the 6H-SiC – SiO<sub>2</sub> interface was examined by photoemission. The VBM was observed to shift after oxidation of the first few monolayers from the surface via O-plasma. The VBM shifted ~1.9 eV lower than the bulk SiC. This was important to observe the blocking characteristics of the oxide on SiC. The conduction band characteristics were extrapolated from  $\Delta VBM$  and  $\Delta\chi$  of the SiC and SiO<sub>2</sub>.

#### E. Future Work

C-V and I-V testing of the oxides on SiC and the Si on SiC in order to examine the interface characteristics. XPS to examine the stoichiometry of the oxide and silicon interfaces. Previous experiments will be repeated on different reconstructions of the SiC.

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